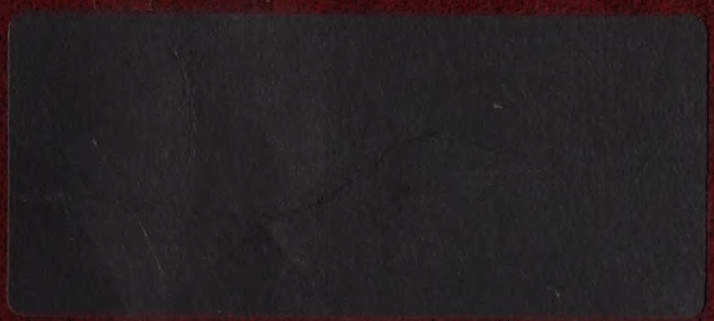
Instruction manual



DATA I/O

Programming systems for tomorrow... today

PROM PROGRAMMER
Program Card Set
909/919-1268-1

025-1268-1 REV E OCT 80

Copyright © Data I/O Corporation, 1980. All rights reserved.

TABLE OF CONTENTS

SECTION 1. SPECIFICATIONS

1.1 INTRODUCTION 1-1

1.2 CALIBRATION PROGRAM ADAPTER 1-1

1.3 CALIBRATION REQUIREMENTS 1-1

SECTION 2. INSTALLATION

2.1 DIGITAL CARD JUMPERS 2-1

2.2 CARD SET INSERTION 2-1
- 2.2.1 Models 1-5 2-1
- 2.2.2 Models 7 and 9 2-2
- 2.2.3 Systems 17 and 19 2-2

SECTION 3. OPERATION

SECTION 4. CALIBRATION

4.1 INTRODUCTION 4-1

4.2 TEST SET-UP 4-1
- 4.2.1 Models 1-5 4-1
- 4.2.2 Model 9 4-3
- 4.2.3 System 19 4-3

4.3 PROCEDURES FOR CALIBRATION 4-4
- 4.3.1 Check the State of the Start/Stop Line 4-5
- 4.3.2 Set the State of the Start/Stop Line 4-5
- 4.3.3 Set the State of the FWD/REV Line 4-5
- 4.3.4 Load Data onto the DI Bus 4-6
- 4.3.5 Confirm Data on the DO Bus 4-6

4.4 WAVEFORM OBSERVATION 4-7
- 4.4.1 Calibration Equipment Set-up 4-7
- 4.4.2 Test Procedure 4-7
- 4.4.3 Parametric Waveforms 4-9
- 4.4.4 Reject Jumper Reinstallation and Abort Test 4-9

SECTION 5. CIRCUIT DESCRIPTION

5.1 INTRODUCTION 5-1
- 5.1.1 Digital Card 5-1
- 5.1.2 Analog Card 5-1
- 5.1.3 Detailed Circuit Description 5-1

5.2 DIGITAL CARD 5-2
- 5.2.1 Select Gates 5-2
- 5.2.2 Program Memory 5-2
- 5.2.3 Master Clock 5-2
- 5.2.4 Timing Sequence Generator 5-2
- 5.2.5 Mode Controller 5-2
- 5.2.6 Bit Counter 5-3
- 5.2.7 Program and Overprogram Operation 5-3
- 5.2.8 Abort Timer 5-3

5.2.9 Parametric Verify Operation 5-3
5.2.10 Word Limit Gating 5-3

5.3 ANALOG CARD 5-4
5.3.1 Bit Decode and Bit Switch 5-4
5.3.2 Program and Read Current Sources 5-4
5.3.3 Voltage Clamp 5-4
5.3.4 Verify Load 5-4
5.3.5 Comparator and Comparator Reference 5-4
5.3.6 Vcc and Chip Enable Generator 5-4

SECTION 6. SCHEMATICS

LIST OF FIGURES

1-1 Parts included in the a)Programming Pak b)Program Card Set
2-1 Digital Card Jumper Locations
2-2 Installation of Card Set in Model 3 or 5
2-3 Installation of Card Set in Model 7 or 9
2-4 Installation of the Program Card Set in the Programming Pak
4-1 Set-up of Models 1-5 for DC Calibration
4-2 Set-up of Model 9 for DC Calibration
4-3 Set-up of System 19 for DC Calibration
4-4 Analog Card Adjustment Locations
4-5 Calibrator Set-up for the Waveform Observations
5-1 Simplified Block Diagram of Program Card Set
5-2 Block Diagram, 1308 Digital Card
5-3 Analog Card Block Diagram

LIST OF TABLES

1-1 Applications of the Program Card Set
2-1 Customer-Selectable Digital Card Jumpers

SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
FUJITSU				
32x8 AIM	7056	VOH OC	16 PIN	1302-1
32x8 AIM	7051	VOH TS	16 PIN	1302-1
256x4 AIM	7057	VOH OC	16 PIN	1303-1
256x4 AIM	7052	VOH TS	16 PIN	1303-1
512x4 AIM	7058	VOH OC	16 PIN	1303-2
512x4 AIM	7053	VOH TS	16 PIN	1303-2
1024x4 AIM	7059	VOH OC	18 PIN	1305-5
1024x4 AIM	7054	VOH TS	18 PIN	1305-5
1024x8 AIM	7060	VOH OC	24 PIN	1455
1024x8 AIM	7055	VOH TS	24 PIN	1455
INTERSIL				
32x8 AIM	5600	VOH OC	16 PIN	1302-1
32x8 AIM	5610	VOH TS	16 PIN	1302-1
256x4 AIM	5603A	VOH OC	16 PIN	1303-1
256x4 AIM	5623	VOH TS	16 PIN	1303-1
512x4 AIM	5604	VOH OC	16 PIN	1303-2
512x4 AIM	5624	VOH TS	16 PIN	1303-2
512x8 AIM	5605	VOH OC	24 PIN	1304-2
512x8 AIM	5625	VOH TS	24 PIN	1304-2
NIPPON ELECTRIC CO., LTD.				
256x4 AIM	B403D	VOH OC	16 PIN	1303-1
512x8 AIM	B405D	VOH OC	24 PIN	1304-2
512x8 AIM	B425D	VOH TS	24 PIN	1304-2
1024x4 AIM	B406D	VOH OC	18 PIN	1039-3
1024x4 AIM	B426D	VOH TS	18 PIN	1039-3

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

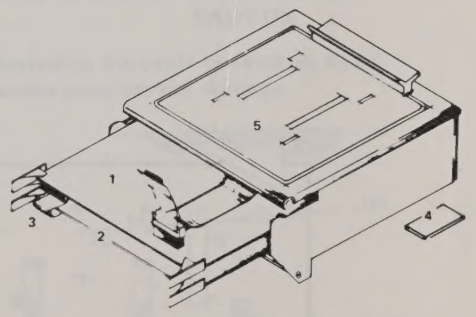
A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).

1.2 PROGRAMMING ALGORITHM

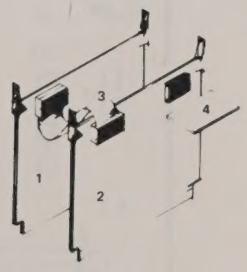
The 909/919-1268-1 Program Card Set compares each bit of each word with the corresponding bit in the programmer RAM. If a bit-to-program is detected, programming pulses are applied to that bit. As soon as the bit verifies, the cardset begins an overprogram sequence, which delivers additional pulses to the bit to insure the programmed bit's reliability. The process is repeated for each bit at that address.

On completion of each word, the programmer is signalled to increment the programmer address. The bit-test, program, verify and overprogram routines are repeated.

When word limit is reached, the programmer reverses direction and steps back down through the addresses, performing a parametric verify of each bit. This involves applying a verify pulse to the bit and checking the bit's ability to source or sink current, depending on whether the bit is programmed high or allowed to remain low.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD	701-1308
2. ANALOG CARD	701-1268-1
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1268-1
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

1.3 CALIBRATOR PROGRAM ADAPTER

The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

1.4 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer-Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP1	Reject	A	
JP2	Parametric Enable	A	
JP3	Word Limit	2048	Selection defaults to socket adapter
JP4		I	

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 and 2 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

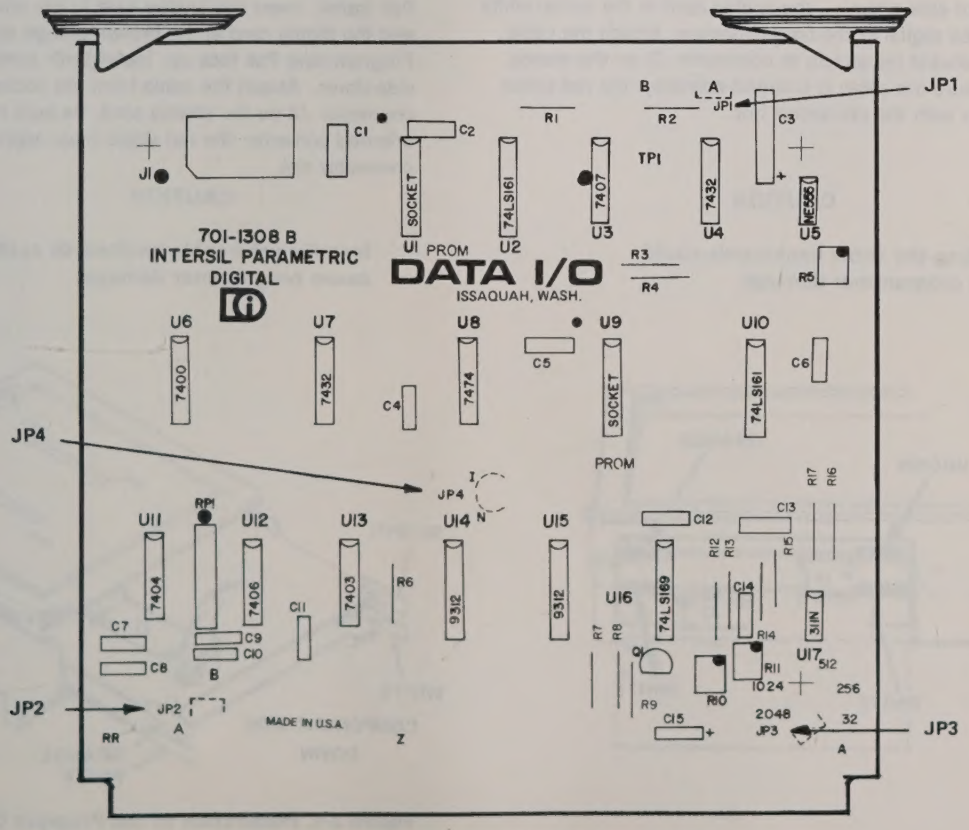


Figure 2-1. Digital Card Jumper Locations

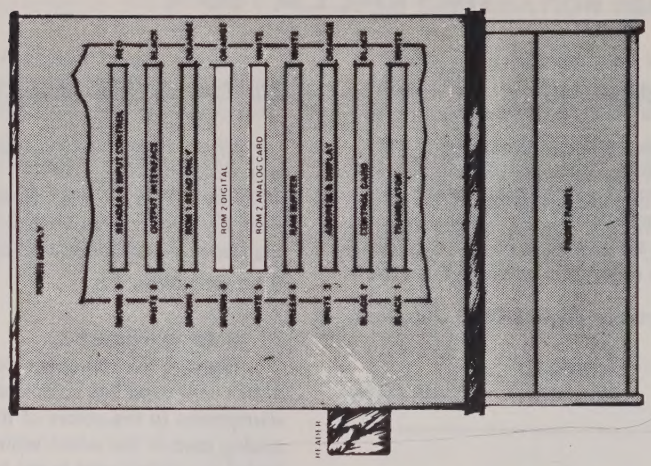


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

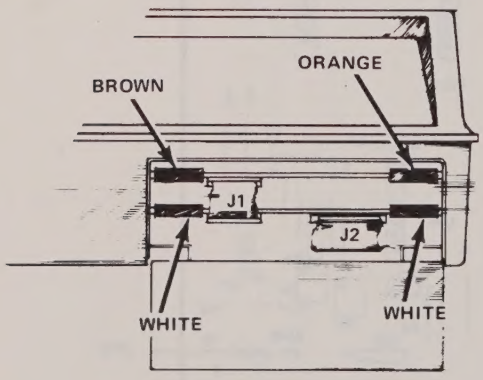


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

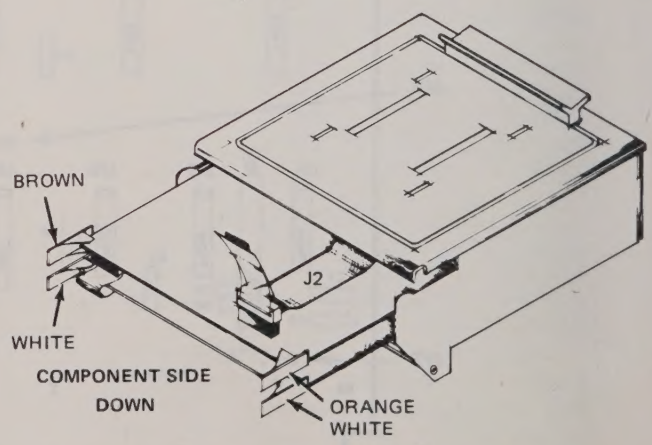


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics. Its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

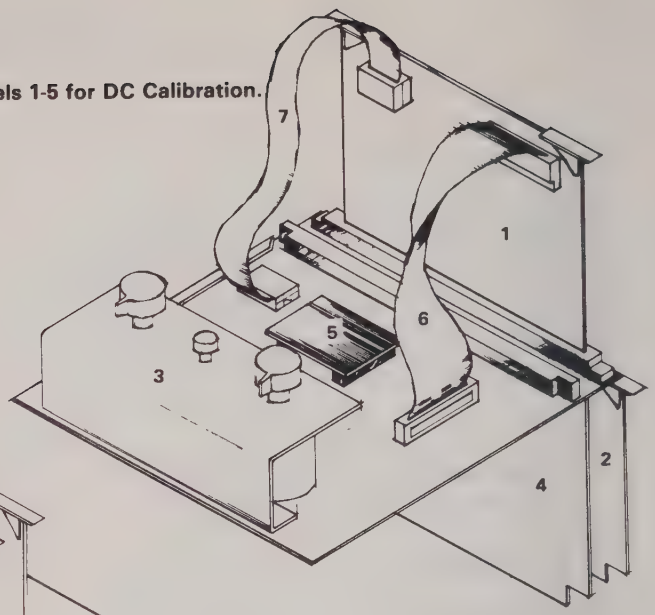
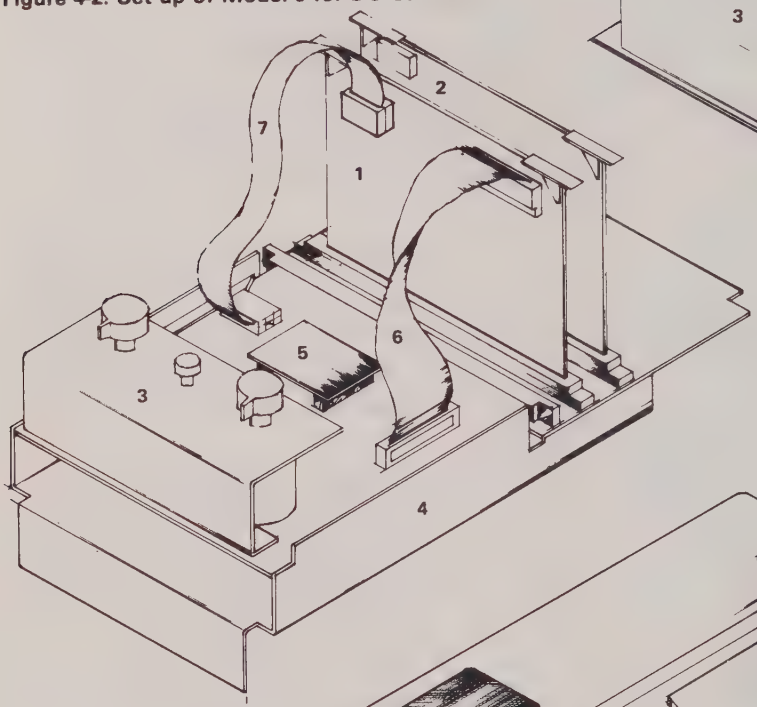
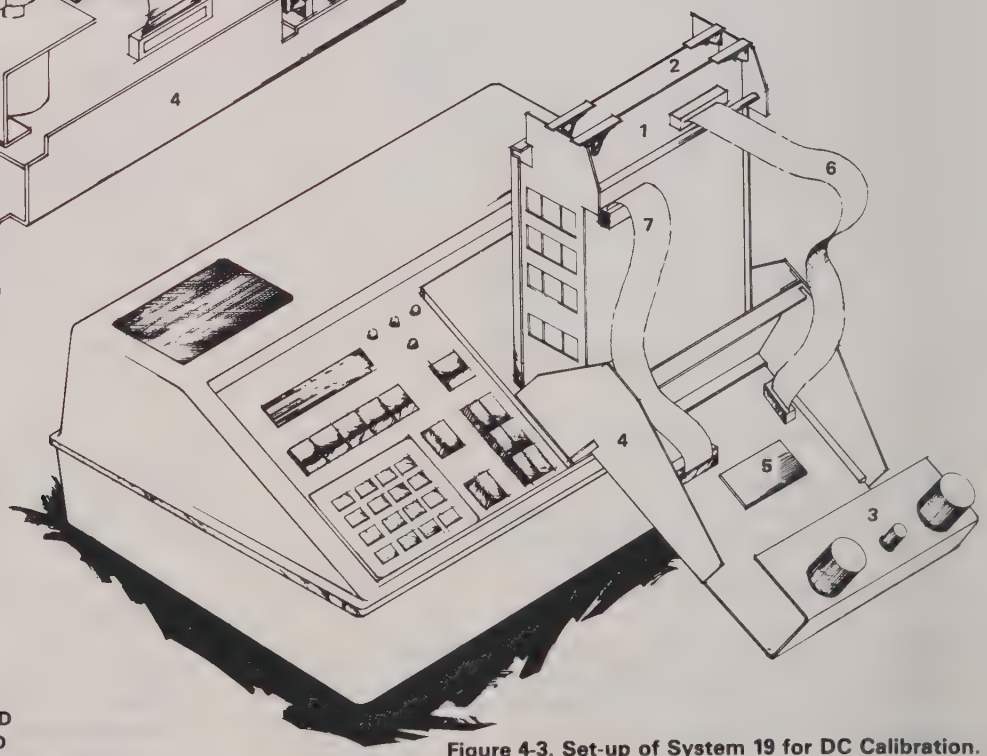


Figure 4-2. Set-up of Model 9 for DC Calibration.





1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

Figure 4-3. Set-up of System 19 for DC Calibration.

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 cn the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE
NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 919-XXXX part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE
To exit calibration, press:
SELECT
CØ (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

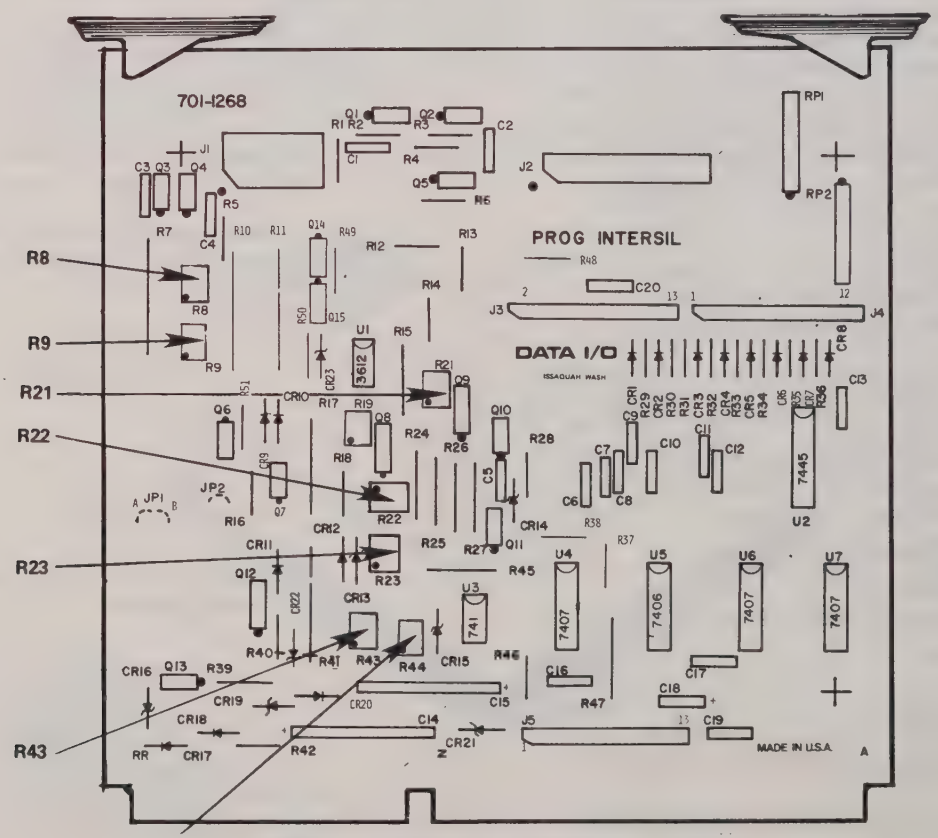


Figure 4-4. Analog Card Adjustment Locations

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1268-1 PROGRAM CARD 909-1268-1
FIXTURE 702-1071 MANUFACTURER AIM GENERIC
PAGE 1 OF 3 PROGRAM ADAPTER 910-1268-1 PROM AIM GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
7-78	C	ECN #2347	KJ	RT
9-78	D	ECN #2400	KJ	RT
11-78	—	ECN #2565	FS	GG
2-11-80	D	ECN #3402	EF	
2-28-80	D	ECN #3406	KB	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
67	15	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments are located on the power supply board. See programmer manual.
67	15	POWER +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	
67	15	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15	
67	15	-9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8	
67	15	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		12.0		16.0	
47	05	VCC VERIFY LOW	2-1	001	01	001	5	1	TP3	R43	4.0	4.1	4.2	*Adjustment Step.*
67	15	VCC PROGRAM (1)	2-2	002	02	002	5	1	TP3	R22	5.0	5.1	5.2	*Adjustment Step.*
47	11	VCC VERIFY HIGH	2-3	003	03	003	5	1	TP3	R23	6.3	6.5	6.7	*Adjustment Step.*
47	11	VCC CURRENT	2-4	003	03	003	6	1	TP3		3.0		6.6	
66	15	REF. LEVEL PROG.	3-1	004	04	004	6	7	U3 P8	R21	6.9	7.0	7.1	Do not press S1. *Adjustment Step.*
66	15	REF. LEVEL PROG.	3-2	004	04	004	6	7	U3 P8		12.4		12.6	Test point located on analog daughter board, 702-1271.
67	15	REF. LEVEL TTL	3-3	005	05	005	7	1	U3 P8		1.2		1.8	
46	05	REF. LEVEL VOL	3-4	006	06	006	7	1	U3 P8		0.75		0.85	
46	11	REF. LEVEL VOH	3-5	007	07	007	7	1	U3 P8		6.9		7.1	
66	FC	READ CURRENT SET	4-1	008	08	010	1	8	TP2	R9	0.195	0.200	0.205	*Adjustment Step.*
66	F4	READ CURRENT OFF	4-2	009	09	011	1	8	TP2		0.0		0.02	
67	15	BIT 8 TTL LOAD	4-3	010	0A	012	3	8	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.
E6	11	BIT 8 VOH LOAD	4-4	011	0B	013	2	8	TP3		0.5		1.5	Confirm bits 1 - 7 ON (HEX 7F) on DO Bus.
67	15	BIT 7 TTL LOAD	4-5	010	0A	012	3	9	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.
E6	11	BIT 7 VOH LOAD	4-6	011	0B	013	2	9	TP3		0.5		1.5	Confirm bits 1 - 6 and 8 ON (HEX BF) on DO Bus.
67	15	BIT 6 TTL LOAD	4-7	010	0A	012	3	10	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.
E6	11	BIT 6 VOH LOAD	4-8	011	0B	013	2	10	TP3		0.5		1.5	Confirm bits 1 - 5, 7 and 8 ON (HEX DF) on DO Bus.
67	15	BIT 5 TTL LOAD	4-9	010	0A	012	3	11	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.
E6	11	BIT 5 VOH LOAD	4-10	011	0B	013	2	11	TP3		0.5		1.5	Confirm bits 1 - 4 and 6 - 8 ON (HEX EF) on DO Bus.
67	15	BIT 4 TTL LOAD	4-11	010	0A	012	3	12	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.
E6	11	BIT 4 VOH LOAD	4-12	011	0B	013	2	12	TP3		0.5		1.5	Confirm bits 1 - 3 and 5 - 8 ON (HEX F7) on DO Bus.
67	15	BIT 3 TTL LOAD	4-13	010	0A	012	3	23	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.
E6	11	BIT 3 VOH LOAD	4-14	011	0B	013	2	23	TP3		0.5		1.5	Confirm bits 1, 2 and 4 - 8 ON (HEX FB) on DO Bus.
67	15	BIT 2 TTL LOAD	4-15	010	0A	012	3	22	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.

COMMENTS
- Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENTS below
- Switch S1 must be depressed for accurate readings.
- CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CALIBRATION CHART 017-1268-1

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	
E6	11	BIT 2 VOH LOAD	4-16	011	0B	013	2	22	TP3		0.5		1.5	Confirm bits 1 and 3 - 8 ON (HEX FD) on DO Bus.
67	15	BIT 1 TIL LOAD	4-17	010	0A	012	3	21	TP3		1.0		2.0	Confirm all bits OFF (HEX 00) on DO Bus.
E6	11	BIT 1 VOH LOAD	4-18	011	0B	013	2	21	TP3		0.5		1.5	Confirm bits 2 - 8 ON (HEX FE) on DO Bus.
67	15	$\overline{CE}$ PROGRAM (2)	5-1	012	0C	014	5	5	TP3		4.8		5.5	
67	17	$\overline{CE}$ VERIFY	5-2	013	0D	015	10	5	TP3		0.0		0.4	
24	FC	CE PROGRAM/VERIFY	5-3	014	0E	016	3	6,7	TP3		1.0		2.0	(2 Steps) CAUTION: See NOTE 1 for Step 5-3 through 6-3.
24	FC	BIT 8 PROG, I OUT SET	6-1	014	0E	016	1	8	TP2	R8	1.9	2.0	2.1	*Adjustment Step.*
24	FC	BIT 8 PROG, V CLAMP SET	6-2	014	0E	016	6	7	U3 P7	R44	31.5	32.0	32.5	Adjustment Step.
24	FC	BIT 8 PROG, V CLAMP	6-3	014	0E	016	7	7	U3 P7	R44	27.5		28.5	*Adjustment Step.* Test point for steps 6-2 and 6-3 located on analog daughter board
46	EC	BIT 8 VERIFY, V CLAMP (VOL)	6-4	015	0F	017	3	8	TP3		4.5		6.5	
46	F8	BIT 8 VERIFY, V CLAMP (VOH)	6-5	016	10	020	3	8	TP3		7.2		8.8	
66	DC	BIT 8 DESELECT	6-6	017	11	021	1	8	TP2		0.0		0.02	
24	DC	BIT 7 I OUT	6-7	018	12	022	1	9	TP2		1.9		2.1	CAUTION: See NOTE 1.
24	DC	BIT 7 V CLAMP	6-8	018	12	022	3	9	TP3		27.5		28.5	
66	BC	BIT 7 DESELECT	6-9	019	13	023	1	9	TP2		0.0		0.02	
24	BC	BIT 6 I OUT	6-10	020	14	024	1	10	TP2		1.9		2.1	CAUTION: See NOTE 1.
24	BC	BIT 6 V CLAMP	6-11	020	14	024	3	10	TP3		27.5		28.5	
66	9C	BIT 6 DESELECT	6-12	021	15	025	1	10	TP2		0.0		0.02	
24	9C	BIT 5 I OUT	6-13	022	16	026	1	11	TP2		1.9		2.1	CAUTION: See NOTE 1.
24	9C	BIT 5 V CLAMP	6-14	022	16	027	3	11	TP3		27.5		28.5	
66	7C	BIT 5 DESELECT	6-15	023	17	027	1	11	TP2		0.0		0.02	
24	7C	BIT 4 I OUT	6-16	024	18	030	1	12	TP2		1.9		2.1	CAUTION: See NOTE 1.
24	7C	BIT 4 V CLAMP	6-17	024	18	030	3	12	TP3		27.5		28.5	
66	5C	BIT 4 DESELECT	6-18	025	19	031	1	12	TP2		0.0		0.02	
24	5C	BIT 3 I OUT	6-19	026	1A	032	1	23	TP2		1.9		2.1	CAUTION: See NOTE 1.
24	5C	BIT 3 V CLAMP	6-20	026	1A	032	3	23	TP3		27.5		28.5	
66	3C	BIT 3 DESELECT	6-21	027	1B	033	1	23	TP2		0.0		0.02	
24	3C	BIT 2 I OUT	6-22	028	1C	034	1	22	TP2		1.9		2.1	CAUTION: See NOTE 1.
24	3C	BIT 2 V CLAMP (4)	6-23	028	1C	034	3	22	TP3		27.5		28.5	
66	1C	BIT 2 DESELECT	6-24	029	1D	035	1	22	TP2		0.0		0.02	
24	1C	BIT 1 I OUT	6-25	030	1E	036	1	21	TP2		1.9		2.1	CAUTION: See NOTE 1.
24	1C	BIT 1 V CLAMP (3)	6-26	030	1E	036	3	21	TP3		27.5		28.5	

NOTE:

1. Do not leave programmer at this word count or S1 depressed for extended periods.

CALIBRATION CHART 017-1268-1

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
66	FC	BIT 1 DESELECT	6-27	031	1F	037	1	21	TP2		0.0		0.02
67	15	ADDRESS TEST VIL, A0 (5)	7-1	682	2AA	1252	7	20	TP3		0.0		0.4
67	15	ADDRESS TEST VIH, A1	7-2	682	2AA	1252	7	19	TP3		4.8		5.15
67	15	ADDRESS TEST VIL, A2	7-3	682	2AA	1252	7	18	TP3		0.0		0.4
67	15	ADDRESS TEST VIH, A3	7-4	682	2AA	1252	7	17	TP3		4.8		5.15
67	15	ADDRESS TEST VIL, A4	7-5	682	2AA	1252	7	16	TP3		0.0		0.4
67	15	ADDRESS TEST VIH, A5	7-6	682	2AA	1252	7	15	TP3		4.8		5.15
67	15	ADDRESS TEST VIL, A6	7-7	682	2AA	1252	7	14	TP3		0.0		0.4
67	15	ADDRESS TEST VIH, A7	7-8	682	2AA	1252	7	13	TP3		4.8		5.15
67	15	ADDRESS TEST VIL, A8	7-9	682	2AA	1252	7	2	TP3		0.0		0.4
67	15	ADDRESS TEST VIH, A9	7-10	682	2AA	1252	7	3	TP3		4.8		5.15
67	15	ADDRESS TEST VIL, A10	7-11	682	2AA	1252	7	4	TP3		0.0		0.4
66	9C	ADDRESS TEST VIH, A0	7-12	1365	555	2525	7	20	TP3		4.8		5.15
66	9C	ADDRESS TEST VIL, A1	7-13	1365	555	2525	7	19	TP3		0.0		0.4
66	9C	ADDRESS TEST VIH, A2	7-14	1365	555	2525	7	18	TP3		4.8		5.15
66	9C	ADDRESS TEST VIL, A3	7-15	1365	555	2525	7	17	TP3		0.0		0.4
66	9C	ADDRESS TEST VIH, A4	7-16	1365	555	2525	7	16	TP3		4.8		5.15
66	9C	ADDRESS TEST VIL, A5	7-17	1365	555	2525	7	15	TP3		0.0		0.4
66	9C	ADDRESS TEST VIH, A6	7-18	1365	555	2525	7	14	TP3		4.8		5.15
66	9C	ADDRESS TEST VIL, A7	7-19	1365	555	2525	7	13	TP3		0.0		0.4
66	9C	ADDRESS TEST VIH, A8	7-20	1365	555	2525	7	2	TP3		4.8		5.15
66	9C	ADDRESS TEST VIL, A9	7-21	1365	555	2525	7	3	TP3		0.0		0.4
66	9C	ADDRESS TEST VIH, A10	7-22	1365	555	2525	7	4	TP3		4.8		5.15
66	9C	GROUND CHECK	8-1	341	155	525	8	24	TP3		0.0		0.08

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 — 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 — 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5:	Observe the START and STOP indicators.
Model 9:	Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.
System 19:	Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5:	Press the START/STOP key.
Model 9:	a. Press KEYBOARD to stop. b. Press EXECUTE to start.
System 19:	a. To set the programmer in START, press KEYBD, ENTER and START. b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5:	Press the FWD key or the REV key.
Model 9:	See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.
Revision "A" Software:	Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify: a. Ground J1-16 on the analog card. b. Press LOAD. c. Press EXECUTE. d. Press KEYBOARD. e. Key in data — Ø hex — at address ØØ1. f. Press VERIFY. g. Press EXECUTE. The programmer will mis-verify

at the address containing data and will STOP in FWD.

h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.) When using a Model 9, always key in the hex data in parentheses to be sure that the correct data is placed on the DI bus.

Revision "A" Software: Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in hex data called out in parentheses on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software: With the KEYBOARD indicator illuminated and all the others OFF, use the hex keypad to key in hex data called out in parentheses on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the hex data in parentheses into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5: Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF. Ignore the hex data on the chart.

Model 9: With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19: With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Remove the digital card from the card slot.

c. Check the Timing Diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

d. Remove JP4 on the digital card. (Refer to Figure 2-1.) Reinstall it in position "N".

e. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

f. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

g. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the Timing Diagram. Connect an input probe to TP3 on the calibrator.

h. Reinstall the digital card in the slot from which it was removed.

i. Check the NOTES column on the Timing Diagram to determine whether the Program Card Set defaults to VOH or VOL for calibration. If and only if the card set defaults to VOH, ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1 — 5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the Timing Diagram specifies the correct polarity. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresss:

Models 1 — 5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data "Ø1" at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the Timing Diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets. Return to address Ø.

4. Select the PROGRAM mode:

Models 1 — 5, press:	RESET PROGRAM AUTO RAM-ROM2

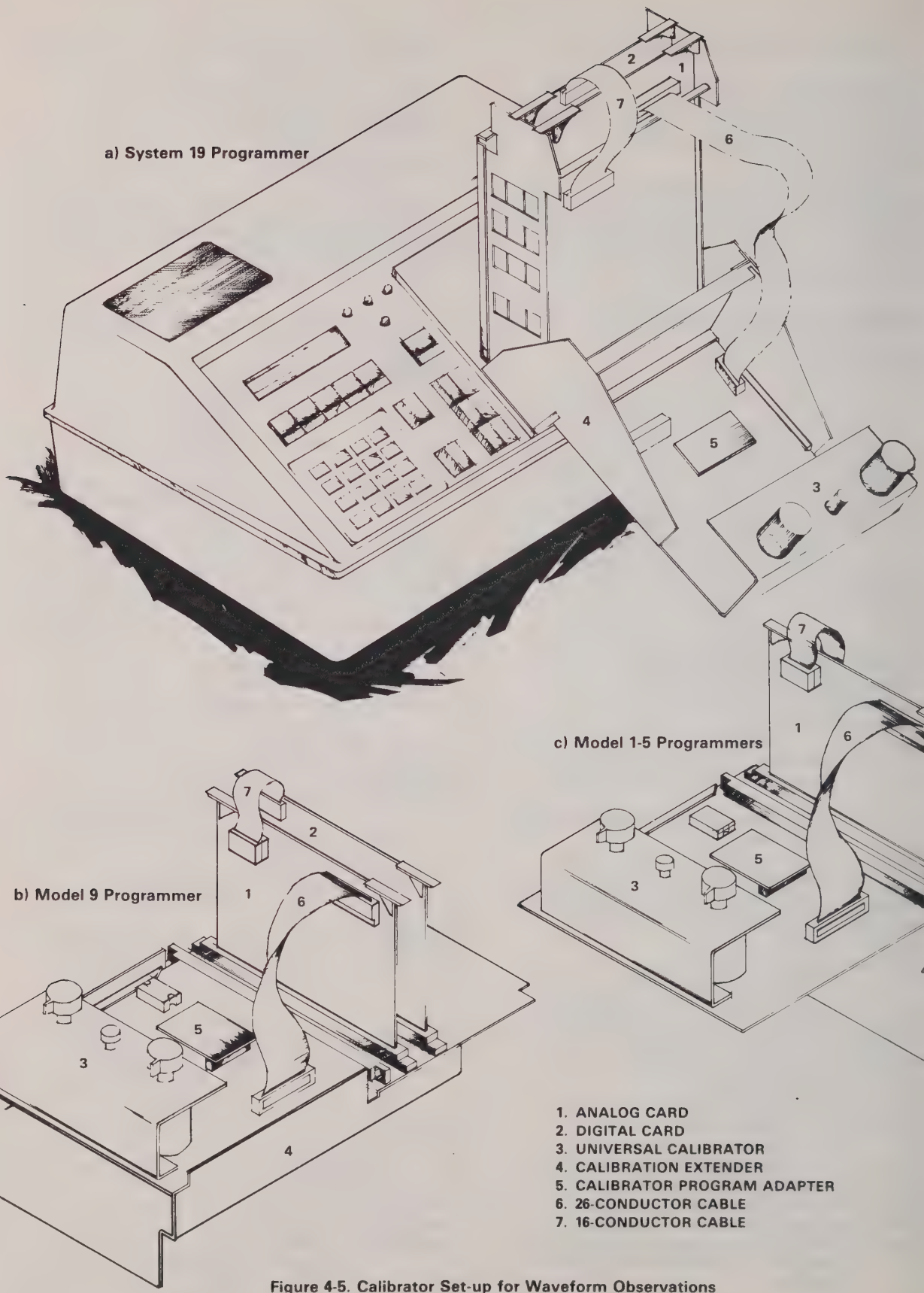
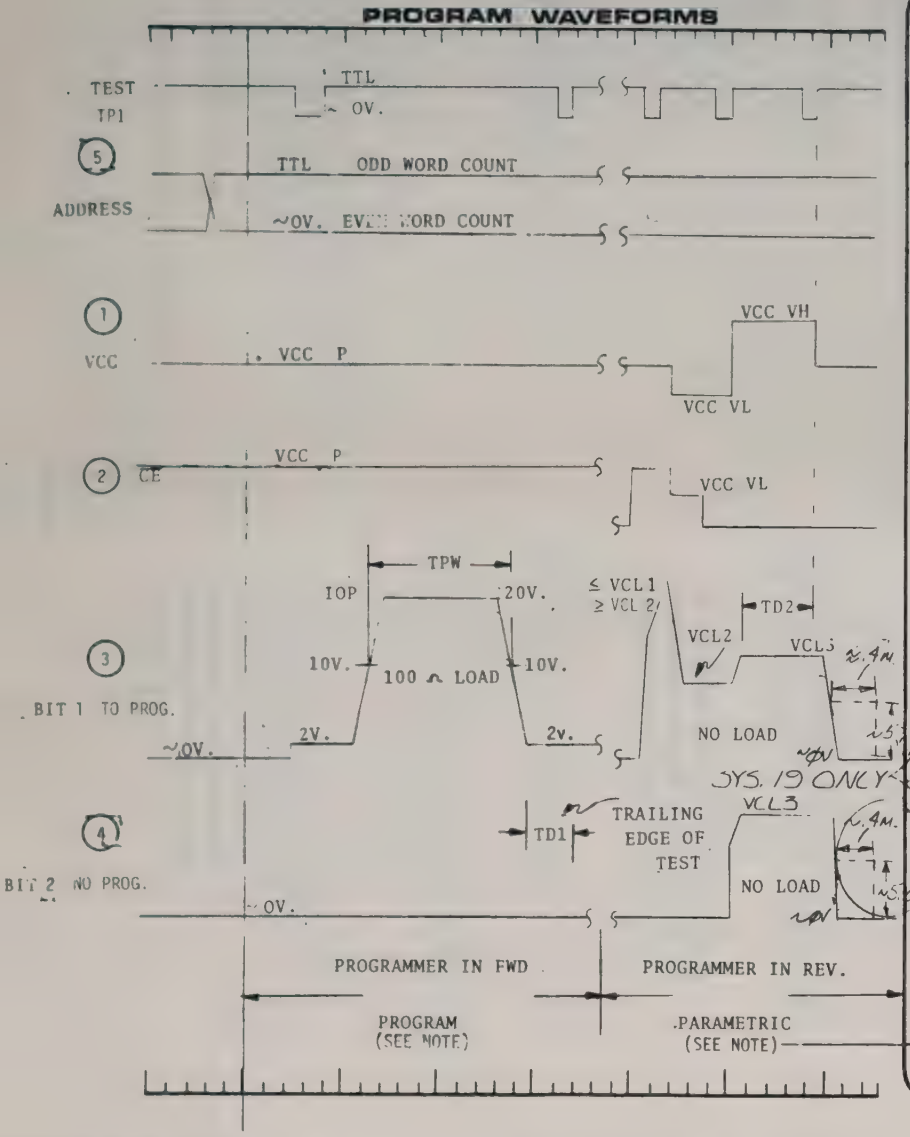


Figure 4-5. Calibrator Set-up for Waveform Observations

2-80	B	Ecn #3496	KB	2-79	-	ECN #2594	FS	
10-80	B	ECN #3009	CF	9-79	-	ECN # 3179		

DATE	SYM	REVISION RECORD	DR
1/77	A	RELEASE	
2/21	-	CN# 1120	
7-78	B	CN# 2347	
9-78	-	CN# 2454	

PROGRAM WAVEFORMS



NOTES

For calibration, the card set polarity defaults to "OH"

ABORT TIMER = 10 ± 2 MS

PROGRAMMER CURRENT (IOP) = 200 ± 10 MA DUTY CYCLE = 75 ± 5%

VERIFY CURRENT (IOV) = 20 ± 0.5 MA

CLAMP VOLTAGE

PROGRAM (32x8) VCL1 = 32 ± 0.5V.
PROGRAM VCL1 = 28 ± 0.5V.
VERIFY (VOL) VCL2 = 5.5 ± 1V.
VERIFY (VOH) VCL3 = 8.0 ± 1V.

REFERENCE VOLTAGE

PROGRAM (32x8) = 12.5 ± 0.1V.
PROGRAM = 7.0 ± 0.1V.
VERIFY (VOL) = 0.8 ± 0.1V.
VERIFY (VOH) = 7.0 ± 0.1V.

VCC VOLTAGE

PROGRAM (VCC P) = 5.25 ± 0.25V.
VERIFY (VCC VL) = 4.1 ± 0.1V.
VERIFY (VCC VH) = 6.5 ± 0.2V.

TPW = 7.5 ± 0.5 µS

TD1 > 1 µS

TD2 ~0.8 MS

OVER PROGRAM = 4 PULSES

FAST CLOCK - ADJ FOR TPW

SLOW CLOCK - ADJ FOR TD2

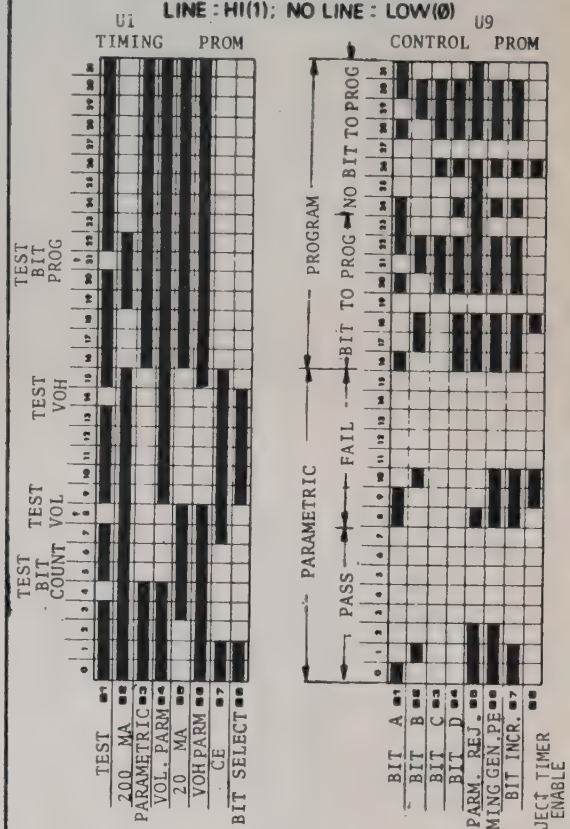
DIGITAL CARD JUMPERS

JP1 = A REJECT
JP2 = A
JP3 = WL = 1024
JP4 = 1

These waveforms correspond to call-outs on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.
NOTE: For program waveforms (3) and (4) (FWD) use S2 position 5; for Parametric waveforms (3) and (4) (REV) use S2 Pos. 7.

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)



DATA I/O ISSAQUAH, WASH.

AIM GENERIC

DRAWN BY P. WALTER

APPROVED BY GJ

TITLE: TIMING DIAGRAM

DATE: 1-5-77

DRAWING NUMBER: 007-1268-1

Model 9, press:	PROGRAM
System 19, press:	SELECT C1 START PROG

5. Initiate waveforms:

Models 1 — 5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1 — 5 and 9, press:	STOP
System 19, press	KEYBD

CAUTION

On completion of observation be sure that JP4 is returned to position "I" before using card set for programming.

4.4.3 PARAMETRIC WAVEFORMS

Refer to the parametric waveforms on the Timing Diagram to perform the following tests. Waveforms are selected by the switch positions as in the "Switch Positions" column on the Calibration Chart.

With programmer power OFF:

1. Install JP4 on digital card to position "I".
2. System 19 only: Remove JP2 on digital card. Ground JP2 pin "A".
3. Using a suitable jumper cable, ground the Read Enable line, digital card J1-16.
4. Model 9 only: set Normal/Invert switch to Normal.
5. Turn programmer power ON.
6. Trigger the scope on TP3 of the Universal Calibrator.
7. Select the Program Mode.

Models 1 — 5, press:	ROM2-ROM2 PROGRAM AUTO
Model 9, press:	PROGRAM
System 19, press:	LOAD START PROGRAM

8. Initiate waveforms:

Models 1 — 5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

The proper waveform will not appear until the programmer reaches word limit and begins its reverse pass through the addresses.

CAUTION

On completion of observation be sure that JP2 is returned to position "A" before using card set for programming.

4.4.4 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

CAUTION

The reject jumper must be reinstalled. Otherwise, the device's programming specifications will be violated, and the programmer and/or cardset may be damaged by a prolonged attempt to program a defective device.

1. Turn the programmer power OFF.

2. Remove the digital card from the card slot.

3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.

4. Reinstall the digital card in the card slot.

5. Ground J1-16.

6. With Universal Calibrator switches set to observe bit-to-program, connect the scope probe to TP3 on the Universal Calibrator.

7. Repeat the key sequence in the Waveform Test Procedure, paragraph 4.4.2 steps 1-5. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort function of the digital card is operative. The System 19 will display ERR 22.

NOTE

The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated. However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram, contact your nearest Data I/O Service Representative for calibration information.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

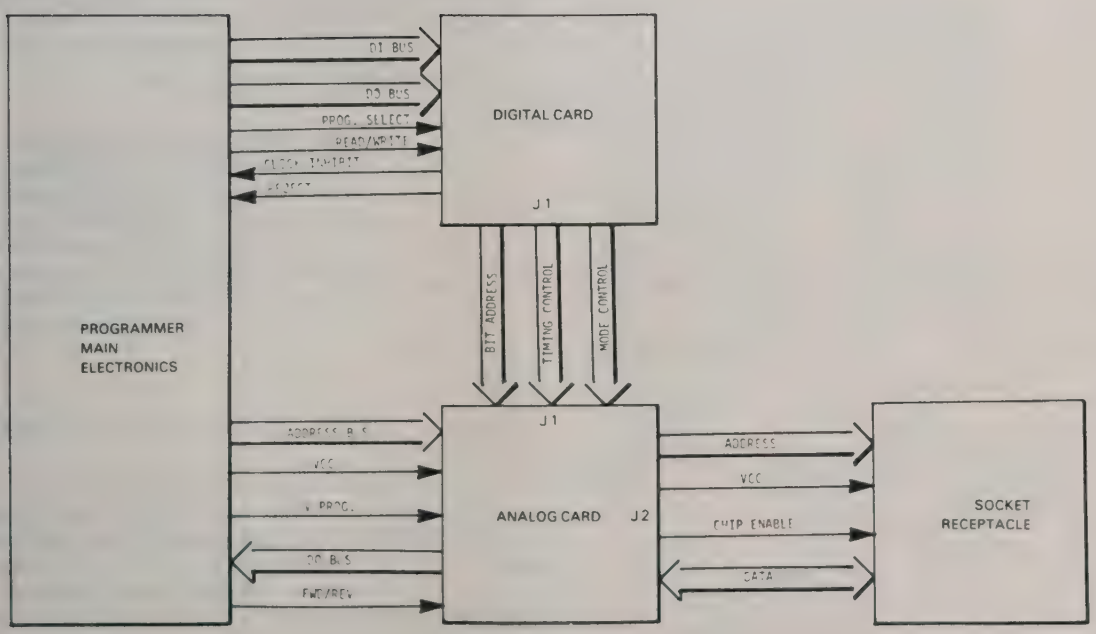


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

Figure 4-2 gives a generalized block diagram of the Digital Card. This diagram shows signal flow, and functional relationships between the blocks, but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) at the rear of this manual for details of circuit connection and operation. The following paragraphs discuss the functions contained in the digital card.

5.2.1 SELECT GATES

The select gates monitor the programmer status lines in order to enable the digital card. Outputs supply data to the Program Memory, and control Verify A and B for 4/8 bit operation and the Abort condition, and are routed to the analog card to control the data bus drivers.

5.2.2 PROGRAM MEMORY

When the digital card is selected for operation, Program Memory will set upon receiving a Write command on line AA. This causes the digital card to begin operation and halts the programmer. Prior to the setting of Program Memory, all counters, memories and timers are initialized.

5.2.3 MASTER CLOCK

The clock is free running with its rate controlled by the high order bit of the Timing Sequence counter. Parallel clocking is used so that all counters and memories (except the Program Memory) receive the same clock pulse.

5.2.4 TIMING SEQUENCE GENERATOR

The Timing Generator consists of a 4-bit counter and a timing ROM. Addressing for the timing ROM is supplied by the sequence counter, which is triggered by the master clock. The combination generates timing signals for analog card control, along with a test pulse used on the digital card (see Timing Diagram).

5.2.5 MODE CONTROLLER

The Mode Controller consists of a 4-bit counter and control ROM. When the Program Memory sets, the sequence counter advances to test, enabling the controller. The controller provides all control to verify and program the desired PROM bits (programmer in FWD) and perform a Parametric Verify while the programmer is in REV.

A test pulse is provided for Bit to Program, Parametric VOL, Parametric VOH, and Bit Counter carry.

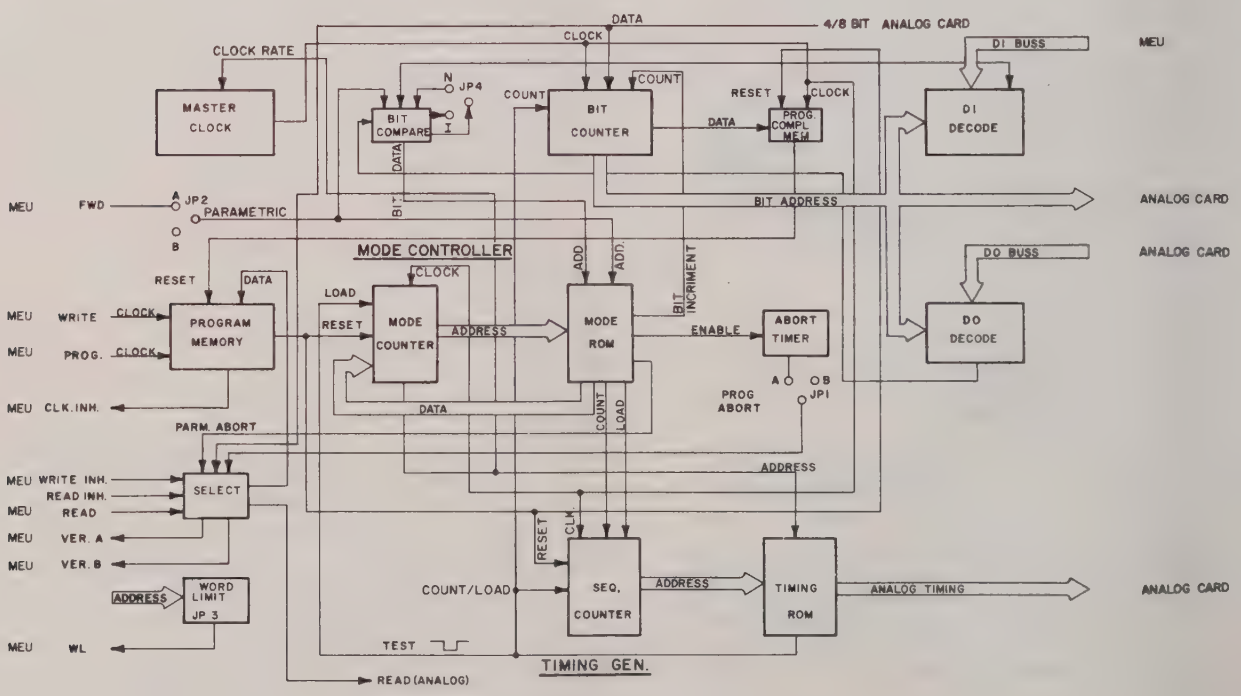


Figure 5-2. Block Diagram, 1308 Digital Card

SOCKET ADAPTER

715-1302-1

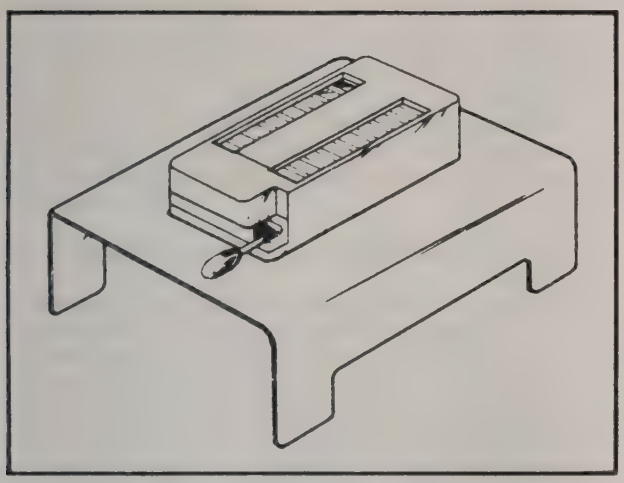


Figure 1. Socket Adapter 715-1302-1.

A Socket Adapter consists of a zero insertion force socket with interface circuitry mounted on an adapter frame. It is used with Data I/O programmers to match programmer electronics to PROM Memory pinout, byte size, and word limit requirements. Refer to the Data I/O Comparison Chart to match device configurations to Socket Adapter part numbers.

In use, the Socket Adapter is installed into a socket receptacle on the programmer front panel. The device to be programmed or read is inserted into the socket (with device pin 1 to upper left) and locked into place by means of a locking arm on the socket.

CAUTION

Do not switch programmer power while a device is installed in the Socket Adapter—voltage transients may cause spurious programming. Do not change devices when a programming operation is occurring (EXECUTE or START indicator illuminated).

STORAGE AND MAINTENANCE

The Socket Adapter should be stored in a location free of dust, excessive moisture, and extremes of temperature and humidity, assuring that top and bottom connectors are protected from possible physical damage.

Periodically inspect each socket contact for accumulation of dirt and debris. Also inspect each contact for smooth opening and closing operation. Dirt and debris can usually be removed with compressed air.

The socket itself is constructed of a polysulfone material and should be cleaned only with methyl alcohol, freon TE, or detergent and water. Do not lubricate. If the socket fails in use, it is most probably caused by mechanical damage to the socket itself, which must be replaced in whole, as replacement parts are not available. Inspect each contact for opening and closing ability to ascertain when the unit should be replaced.

CIRCUIT DESCRIPTION

Figure 2 is a schematic representation of Socket Adapter electronics. Device pinout is shown at the center. Socket pins, which mate with the programmer receptacle, are shown to either side. Looking at the top of the Socket Adapter, device pin one is on the upper left. Looking at the underside of the Socket Adapter, connector pin one is on the upper left. Refer to the analog card schematic in the program card set Instruction Manual to determine signal routing to the connector pins from the analog card.

Decoupling capacitors C10 through C16 bypass voltage transients to ground. Transistor Q1 turns on at device word limit, signalling the programmer.

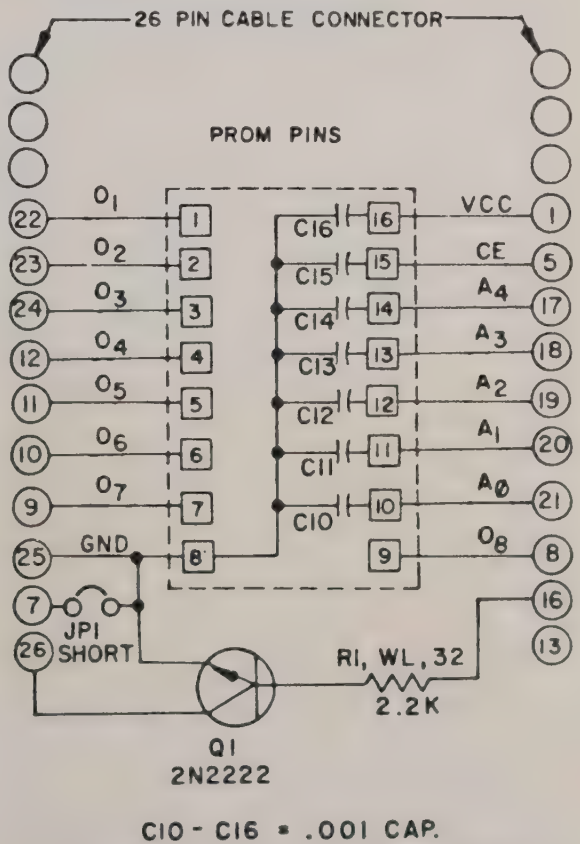


Figure 2. Schematic Diagram, Socket Adapter 715-1302-1.

5.2.6 BIT COUNTER

The Bit Counter counts bit increment pulses arriving from the mode control ROM. The bit counter counts down from either 4 or 8, as determined by the 4/8 bit mode input from the analog card. Outputs from the bit counter address the DO & DI Bus Decoder and are supplied as bit addresses to the analog card. When the Bit Counter reaches zero, its borrow sets the Program Complete Memory and then resets the Program Memory.

5.2.7 PROGRAM AND OVERPROGRAM OPERATION

When test and the DO & DI Decoder outputs yield a bit to program, the controller addresses the timing ROM into high order and allows the sequencer to advance to Program. A program pulse is delivered via the analog card and the sequencer loops back to test. If test still yields a bit to program, the sequencer repeats another Program and bit test sequence. This sequence repeats as long as test yields a bit to progmam and the abort timer has not timed out.

When the sequencer is in high order and test yields no bit to program, the controller allows four program bit test sequences, hence delivering four extra (overprogram) pulses. The controller then addresses the sequencer back into low order, reseting the Abort Timer and incrementing the Bit Counter. The entire sequence is repeated for the next bit in the word.

5.2.8 ABORT TIMER

The Abort Timer measures the time required to program a bit. If programming time is excessive, the timer clocks out, and if JP1 is in position A, the sequencer is halted and a reject is signalled. The controller allows a reject only at test time, therefore stopping the sequencer on test conditions only.

5.2.9 PARAMETRIC VERIFY OPERATION

Following successful programming of the PROM, the Programmer reverses, enabling parametric verify. The sequencer advances to the VOL parametric test. If test and the DO and DI Bus decoders yield a verify (pass), the controller allows the sequencer to advance to the parametric VOH test. If test yields a verify the sequencer loops back to bit increment, incrementing the bit counter, and the sequence is repeated for the next bit. During Parametric Verify the sequencer is held in low order.

If Parametric Test yields a mis-verify (fail), the sequencer is halted and an abort is signalled.

5.2.10 WORD LIMIT GATING

Word limit gates provide the capability for a jumperable Word Limit. The Gate output pulls Word Limit low when the jumper-selected (JP3) address line goes high.

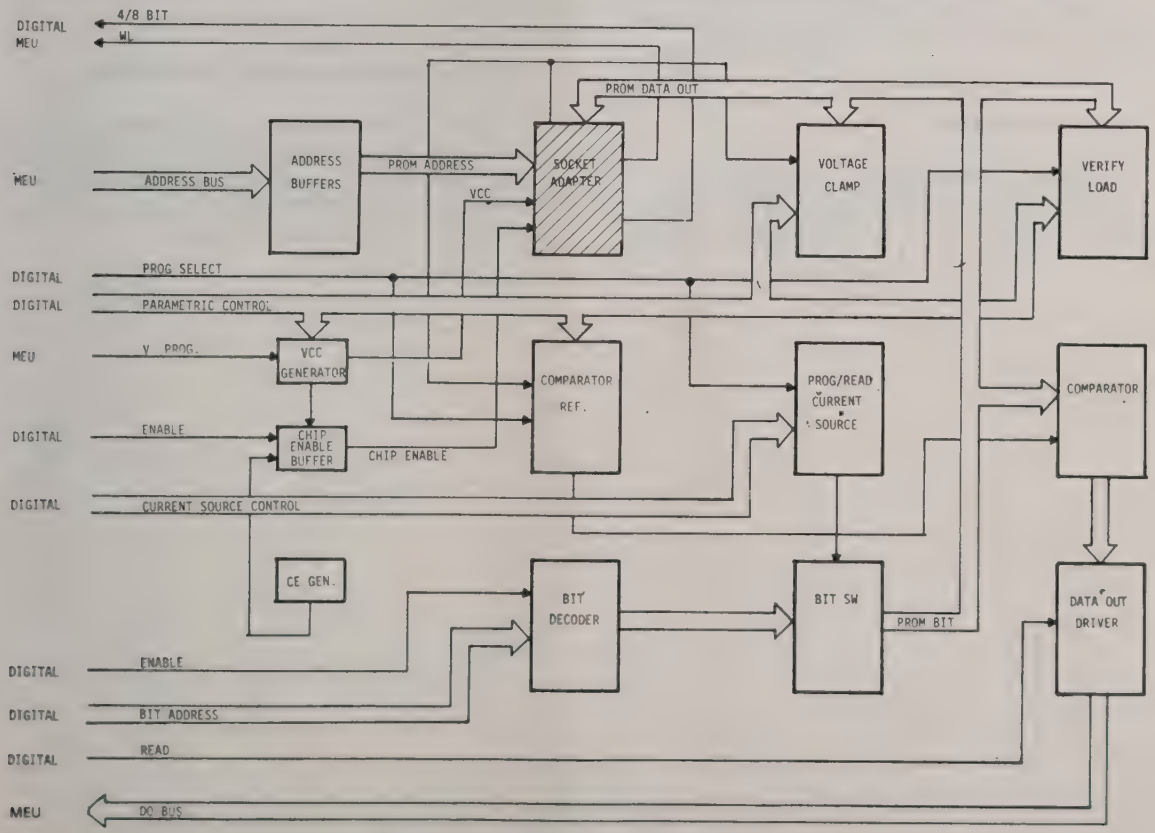


Figure 5-3. Analog Card Block Diagram

5.3 ANALOG CARD

Figure 4-3 gives a generalized block diagram of the analog card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnection information. Refer to the schematics and timing diagram (with truth tables) at the rear of this manual for details of circuit connection and operation. The following paragraphs discuss the functions contained on the analog card.

5.3.1 BIT DECODE AND BIT SWITCH

PROM bits are programmed individually within a given PROM word. Bit information in binary form arrives at J1 on the analog card and is used to drive the Bit Decoder. Decoder outputs enable the appropriate Bit Program Switches to transfer program pulses to the bit lines of the PROM being programmed.

5.3.2 PROGRAM AND READ CURRENT SOURCES

The current sources receive control from the digital card. During Bit Verify, the Read source is routed to the bit switches, and during Program the program source is added to the Read source and routed to the bit switches. The Read source is interrupted during an address change and held for a specified time prior to testing for a bit to program.

5.3.3 VOLTAGE CLAMP

The maximum voltage presented to the bits of the PROM is regulated by the Voltage Clamp. During Read and Program this voltage is set at the specified value, and the clamp is capable of sinking the total Program and Read currents. During Parametric Verify the clamp is set to the specified values for VOL and VOH tests.

5.3.4 VERIFY LOAD

Loading of the PROM bits being verified is controlled by the Verify Load circuit. Parametric VOL and VOH loads are selectively connected to the PROM bit being verified and are disabled during Program. A Read Load is supplied when the device is selected as an input source.

5.3.5 COMPARATOR AND COMPARATOR REFERENCE

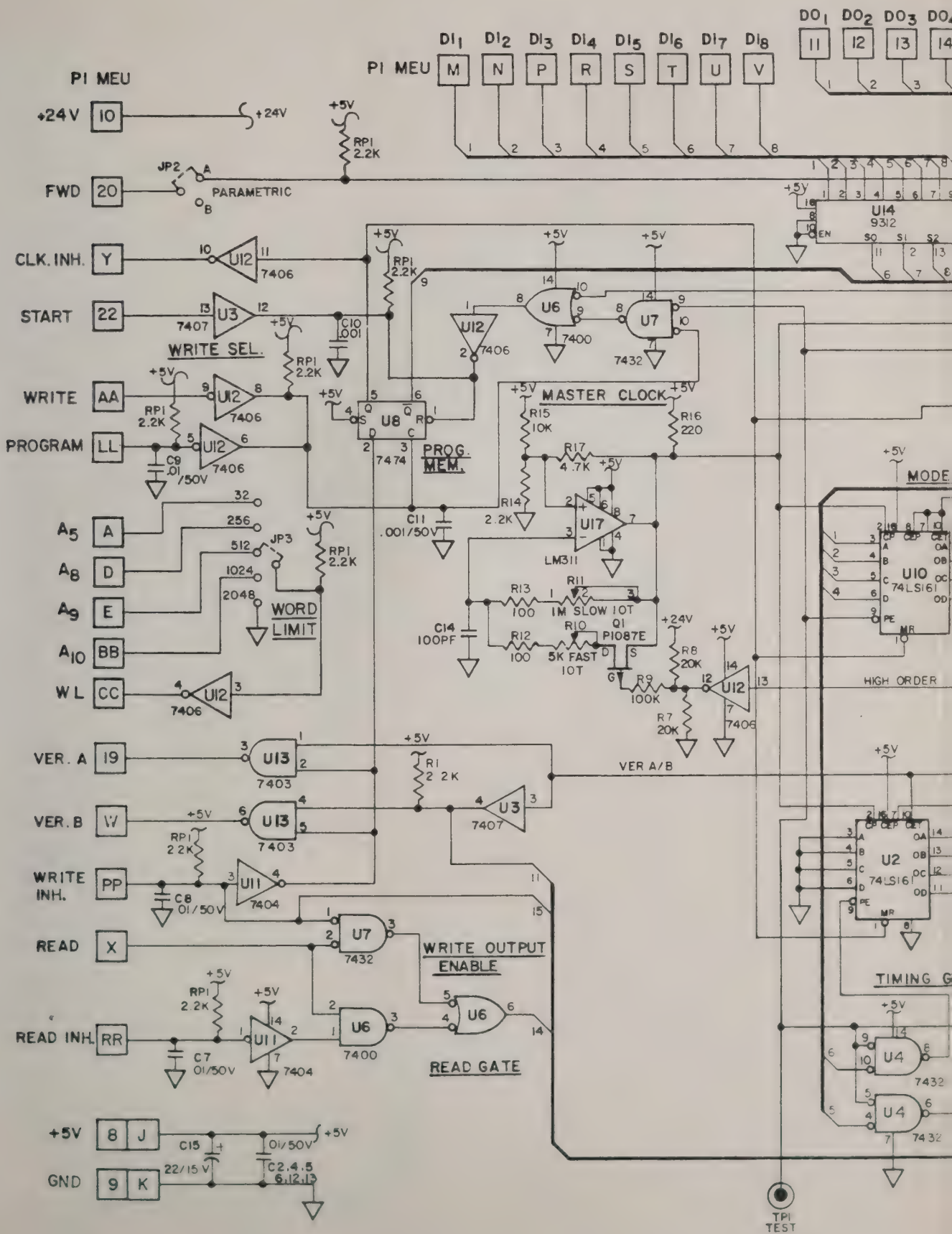
PROM outputs tested during Read, Program and Verify are compared with specified comparator reference levels. Comparator outputs are transferred to the DO Bus when the Read line goes high. This transfer allows the digital card to make a digital comparison of the transferred PROM output (DO Bus) with the programmer DI Bus.

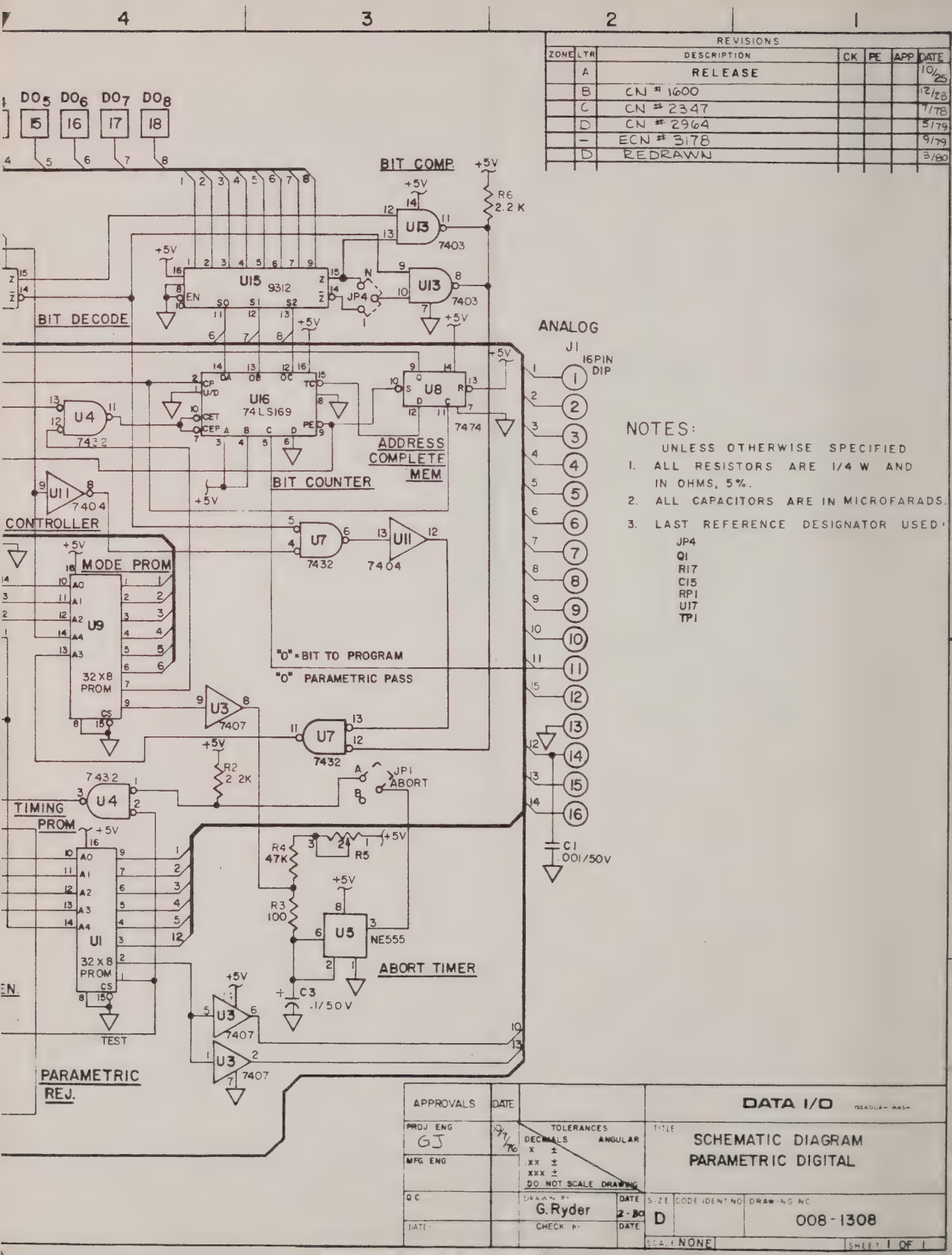
5.3.6 V_{CC} AND CHIP ENABLE GENERATOR

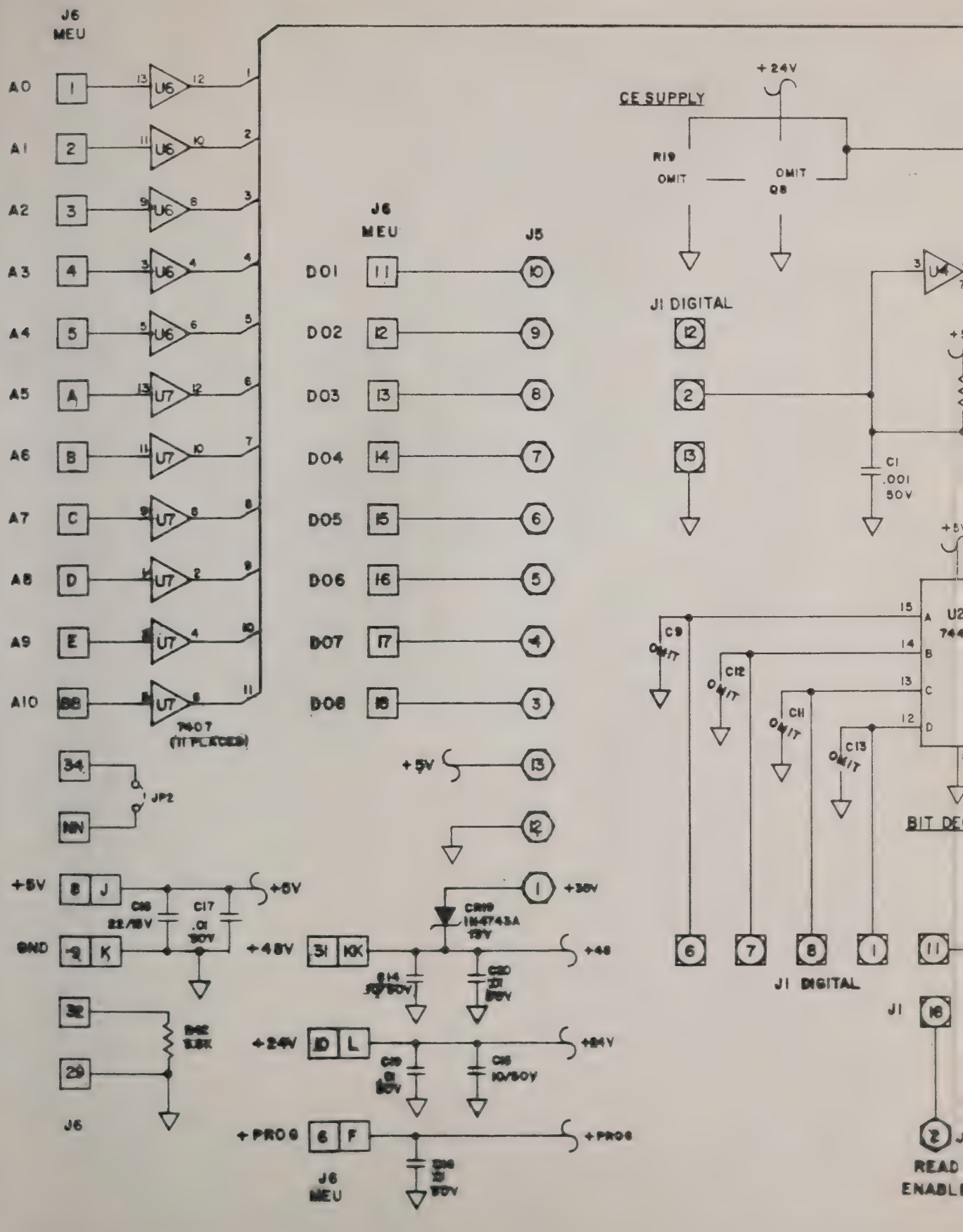
The V_{CC} Generator outputs the specified voltage levels to the PROM during Read, Program and Verify. The CE Generator and buffer output the specified voltage level to the CE input of the PROM during Program and Read. During Verify the CE Input is held low.

SECTION 6
SCHEMATICS

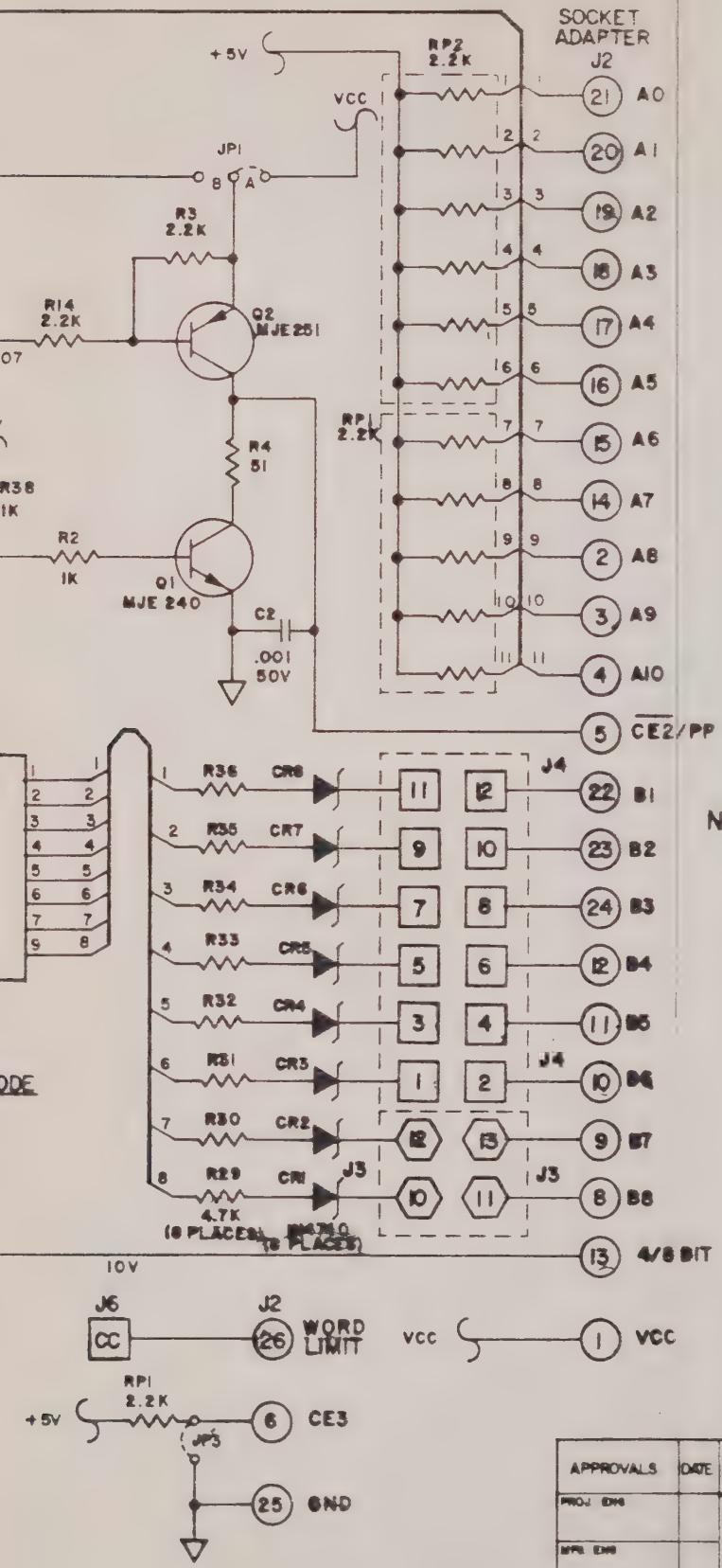
008-1308	Digital Card
008-1268-1	Analog Card
008-1271	Analog Daughter Card
008-1072	Calibration Adapter


PI MEU
+24V 10
FWD 20
JP2
A
B
PARAMETRIC
CLK. INH. Y
START 22
WRITE SEL.
WRITE AA
PROGRAM LL
A5 A
A8 D
A9 E
A10 BB
WL CC
VER. A 19
VER. B W
WRITE INH. PP
READ X
READ INH. RR
+5V 8 J
GND 9 K
RP1 2.2K
U12 7406
U3 7407
U6 7400
U7 7432
U8 7474
PROG. MEM.
C10 .001
C9 .01 /50V
C11 .001/50V
C8 01/50V
C7 01/50V
C15 22/15V
C2,4,5 6,12,13 01/50V
MASTER CLOCK
R15 10K
R16 220
R17 4.7K
R14 2.2K
U17 LM311
R13 100
R11 1M SLOW 10T
R10 5K FAST 10T
R12 100
C14 100PF
Q1 P1087E
R8 20K
R9 100K
R7 20K
JP3
32
256
512
1024
2048
WORD LIMIT
U13 7403
U11 7404
R1 2 2K
VER A/B
WRITE OUTPUT ENABLE
READ GATE
PI MEU M N P R S T U V
DI1 DI2 DI3 DI4 DI5 DI6 DI7 DI8
DO1 DO2 DO3 DO4
11 12 13 14
U14 9312
EN S0 S1 S2
MODE
U10 74LS161
U2 74LS161
HIGH ORDER
TIMING G
U4 7432
TPI TEST


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
A RELEASE 10/25
B CN # 1600 12/28
C CN # 2347 7/78
D CN # 2964 5/79
– ECN # 3178 9/79
D REDRAWN 3/80
DO5 DO6 DO7 DO8
15 16 17 18
BIT COMP
+5V
R6 2.2 K
U13 7403
U15 9312
JP4
BIT DECODE
ANALOG
J1 16PIN DIP
U16 74LS169
U8 7474
U4 7432
ADDRESS COMPLETE MEM
BIT COUNTER
U11 7404
CONTROLLER
U7 7432
MODE PROM
U9 32X8 PROM
"0" = BIT TO PROGRAM
"0" PARAMETRIC PASS
U3 7407
R2 2.2K
JP1 ABORT
TIMING PROM
U1 32X8 PROM
TEST
R4 47K
R5
R3 100
U5 NE555
ABORT TIMER
C3 .1/50V
C1 001/50V
PARAMETRIC REJ.
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
JP4
Q1
R17
C15
RP1
U17
TP1
APPROVALS DATE
PROJ ENG GJ 10/1/76
MFG ENG
QC
DATE
TOLERANCES
DECIMALS ANGULAR
X ±
.XX ±
XXX ±
DO NOT SCALE DRAWING
DRAWN BY G.Ryder DATE 2-80
CHECK BY DATE
DATA I/O
TITLE
SCHEMATIC DIAGRAM
PARAMETRIC DIGITAL
SIZE D
CODE IDENT NO
DRAWING NO 008-1308
SCALE NONE
SHEET 1 OF 1

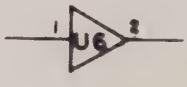

J6
MEU
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
U6
U7
7407
(11 PLACES)
J6
MEU
J5
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
+5V
JP2
+5V
GND
C16
22/15V
C17
.01
50V
+48V
C18
.01
50V
+24V
C19
.01
50V
C20
.01
50V
C14
10/50V
C15
10/50V
+PROG
C21
.01
50V
CR19
1N4743A
13V
+36V
+48
+24V
+PROG
J6
MEU
CE SUPPLY
+24V
R19
OMIT
OMIT
Q8
J1 DIGITAL
C1
.001
50V
C9
OMIT
C12
OMIT
C11
OMIT
C13
OMIT
J1 DIGITAL
J1
READ
ENABL

REVISIONS						
ZONE	LTR	DESCRIPTION	CK	PE	APP	DATE
	G	ECN NO. 3594	BV			3-8

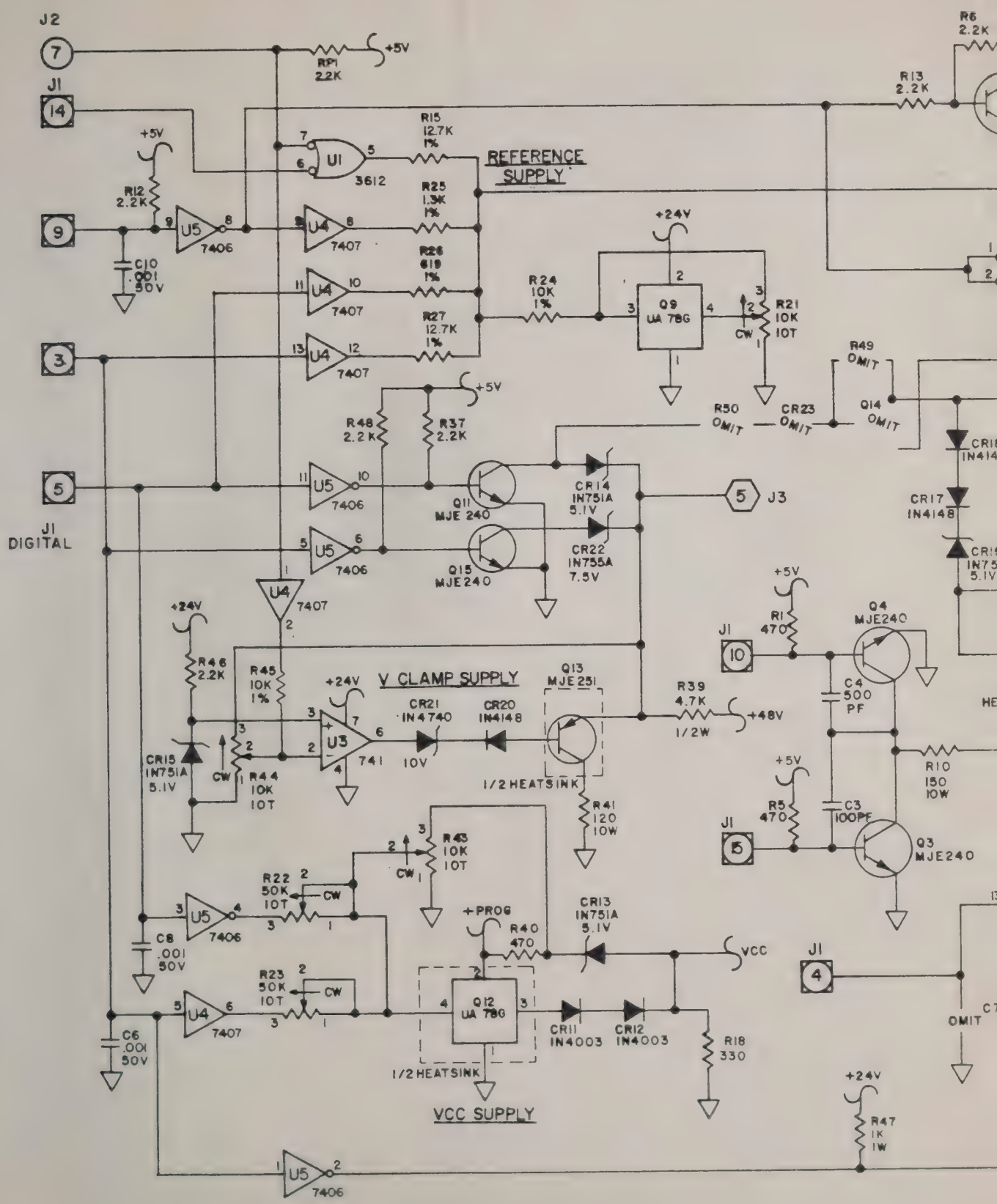


NOTES: UNLESS OTHERWISE SPECIFIED

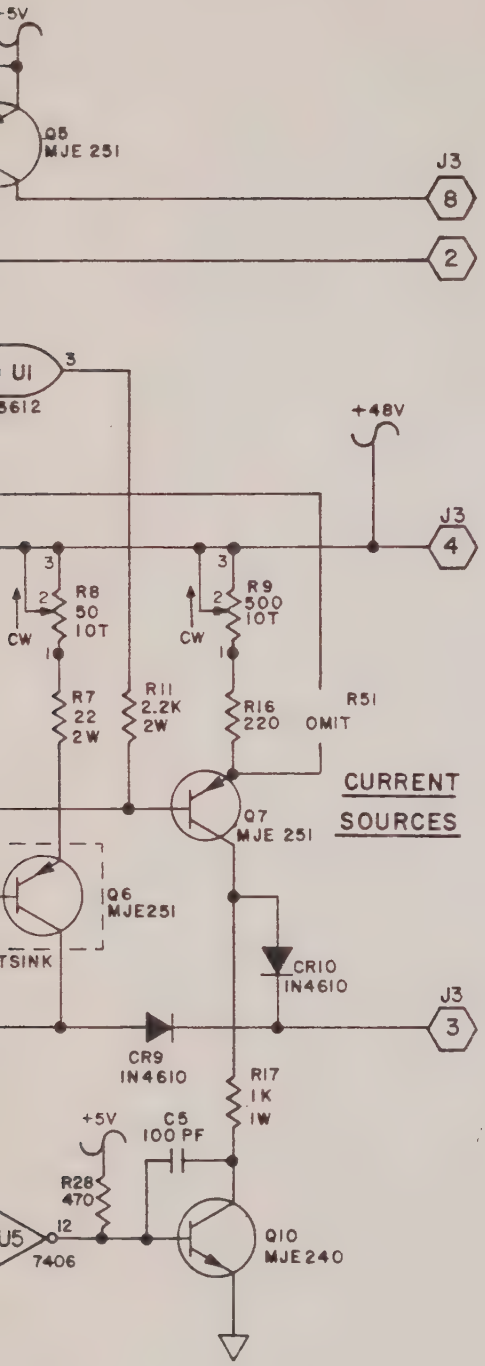
1. ALL RESISTORS ARE 1/4 W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
   C20, CR22, J6, JP3, Q15, R47, U7, RP2
4. UNUSED GATES:



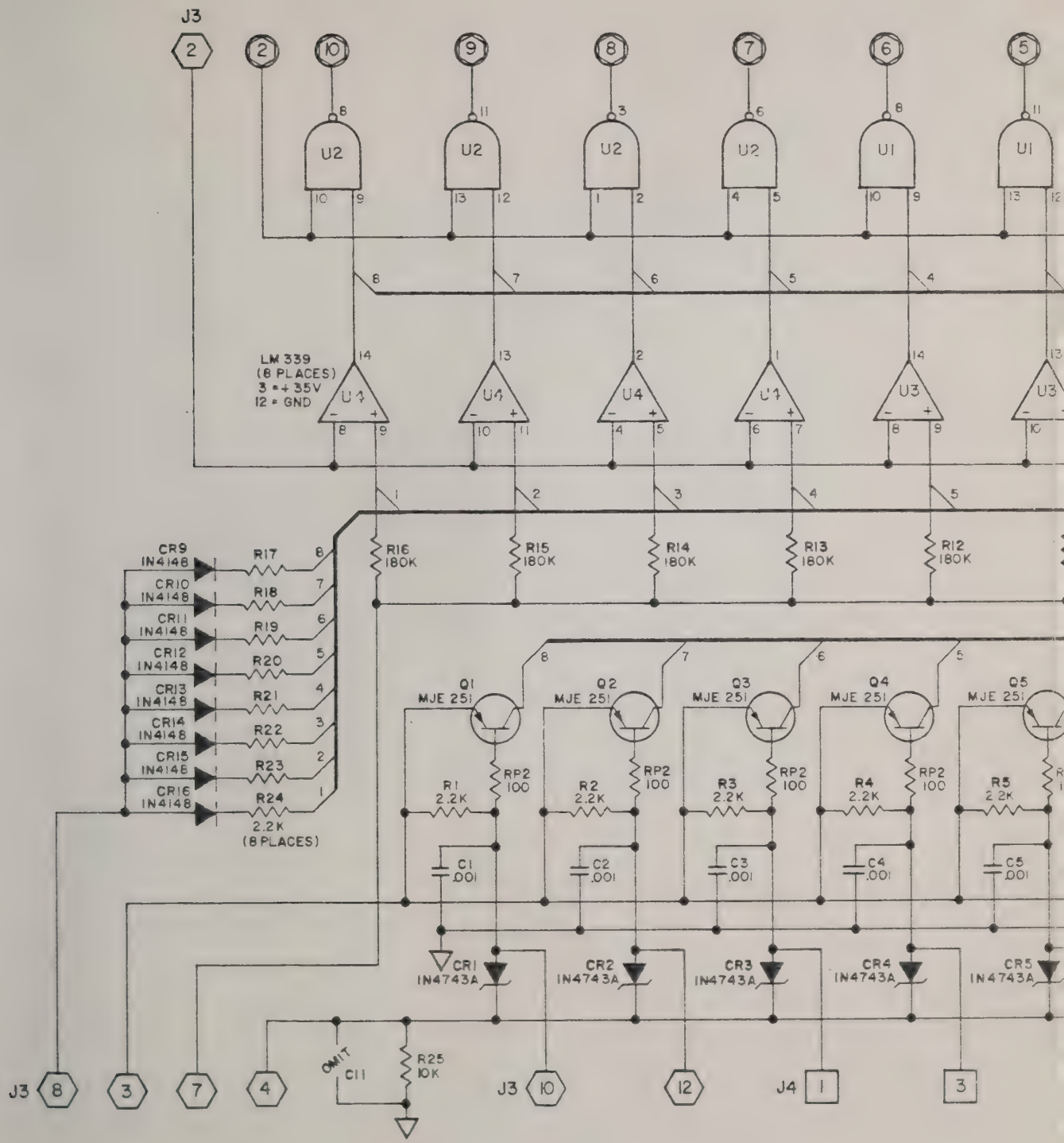
APPROVALS	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
PROJ ENG		TOLERANCES DECIMALS X ± .XX ± .XXX ± ANGULAR DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM AIM GENERIC
MFG ENG			
Q C		DRAWN BY J. OBIE DATE 5/80	SIZE D CODE IDENT NO DRAWING NO 008-1268-1
ENG MGR		CHECKED BY DATE	SCALE - NONE SHEET 1 OF 2


J2
7
J1
14
9
3
5
J1
DIGITAL
RP1
2.2K
+5V
R12
2.2K
C10
.001
50V
U1
3612
R15
12.7K
1%
REFERENCE
SUPPLY
R25
1.3K
1%
R26
619
1%
R27
12.7K
1%
U5
7406
U4
7407
R24
10K
1%
+24V
Q9
UA 78G
R21
10K
10T
CW
R6
2.2K
R13
2.2K
R49
OMIT
R50
OMIT
CR23
OMIT
Q14
OMIT
R48
2.2K
R37
2.2K
Q11
MJE 240
Q15
MJE240
CR14
IN751A
5.1V
CR22
IN755A
7.5V
5
J3
CR16
IN4148
CR17
IN4148
CR18
IN751
5.1V
V CLAMP SUPPLY
R46
2.2K
R45
10K
1%
U3
741
CR21
IN4740
10V
CR20
IN4148
Q13
MJE 251
1/2 HEATSINK
R39
4.7K
1/2W
+48V
R41
120
10W
CR15
IN751A
5.1V
R44
10K
10T
R43
10K
10T
R22
50K
10T
C8
.001
50V
R23
50K
10T
C6
.001
50V
+PROG
R40
470
CR13
IN751A
5.1V
VCC
Q12
UA 78G
CR11
IN4003
CR12
IN4003
R18
330
1/2 HEATSINK
VCC SUPPLY
R47
1K
1W
J1
10
R1
470
Q4
MJE240
C4
500
PF
R10
150
10W
J1
15
R5
470
C3
100PF
Q3
MJE240
J1
4
OMIT

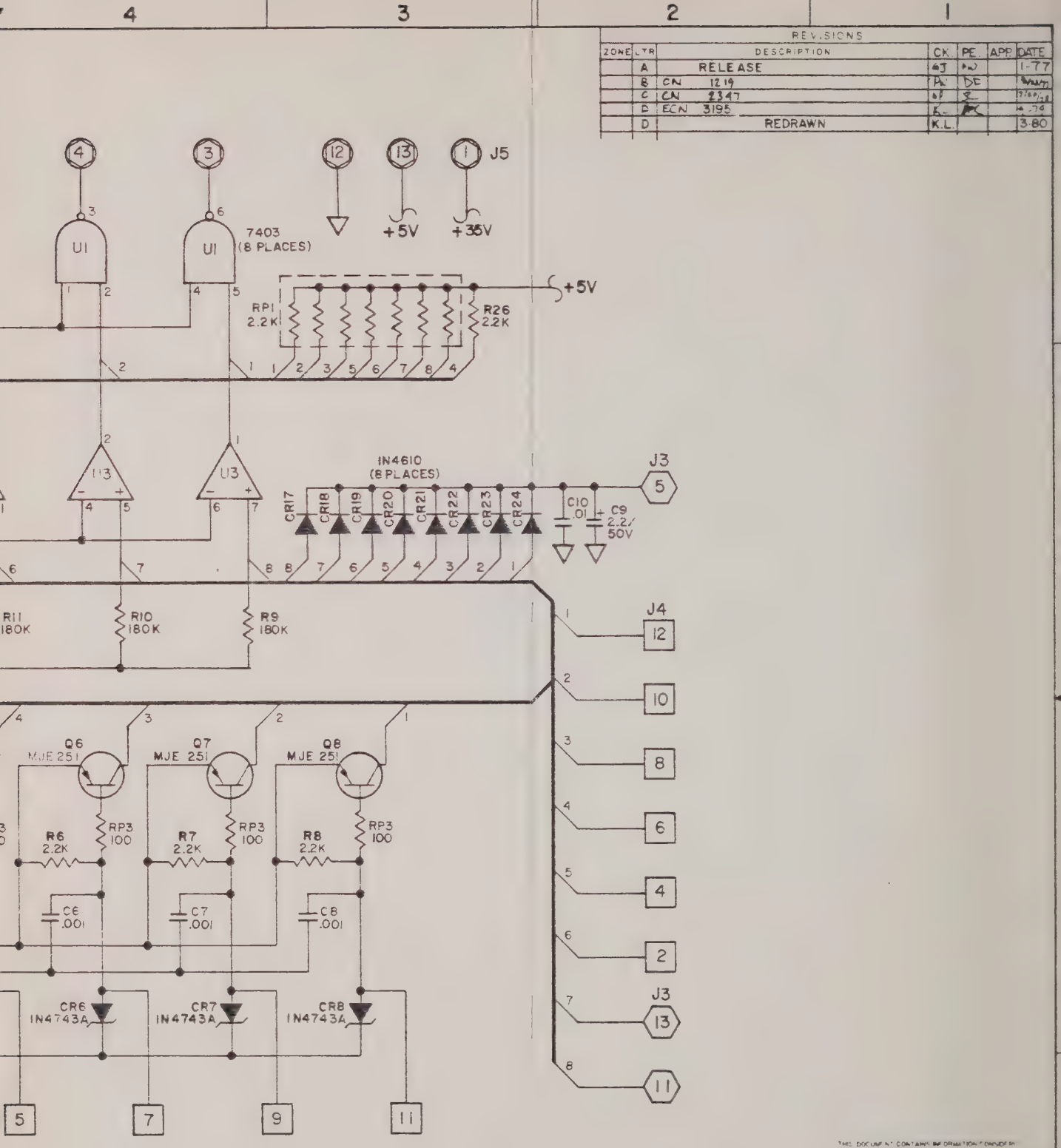
REVISIONS						
ZONE	LTR	DESCRIPTION	CK	PE	APP	DATE
	G	SEE SHT. 1				3-80



APPROVALS	DATE		DATA I/O
PROJ ENG		TOLERANCES DECIMALS ANGULAR x ± .xx ± .xxx ± DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM AIM GENERIC
MFG ENG			
QC		DRAWN BY J.OBIE DATE 3-80	SIZE D CODE IDENT NO DRAWING NO 008-1268-1
ENG MGR		CHECKED BY Kathryn Lang DATE 4-80	SCALE - NONE SHEET 2 OF 2



J3,4,5 ANALOG CARD



THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO DATA I/O CORP. AND SHALL NOT BE REPRODUCED WHOLLY OR IN PART NOR DISCLOSED TO OTHERS WITHOUT THE EXPRESS WRITTEN PERMISSION OF DATA I/O CORP.

APPROVALS: DATE

PROJ ENG VEB 1/SW 4-1

MFG. ENG

QC

ENG MGR

NEXT ASS'

TOLERANCES
DECIMALS ANGULAR
X ±
.XX ±
.XXX ±
DO NOT SCALE DRAWING

DRAWN BY: G. Ryder DATE 2/80

CHECKED DATE

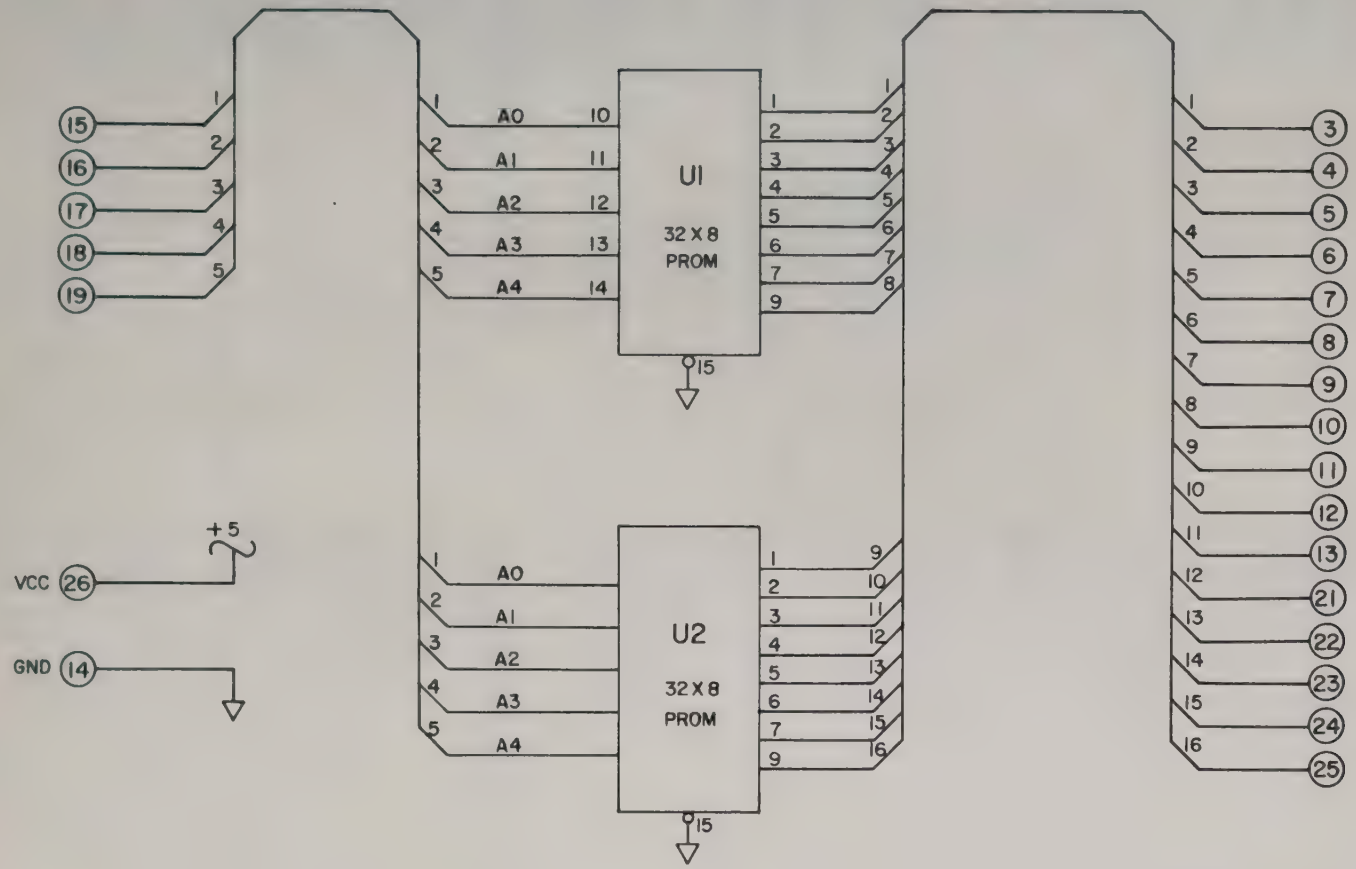
DATA I/O REDMOND, WASH.

TITLE SCHEMATIC DIAGRAM
1268 ANALOG DAUGHTER
BOARD

SIZE D CODE IDENT NO DRAWING NO 008-1271

SHEET 1 OF 1

DATE	SYM	REVISION RECORD	DR	CK
11-13-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL -		SCALE	DRAWN BY G. ROPPE
FRACTIONAL -	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED
ANGULAR -	DATE 10-15-75	DRAWING NUMBER 008-1072	

U.S. and Canada Sales Offices and Representatives
Direct Sales and Service Offices

ALASKA, HAWAII, OREGON, WASHINGTON

Data I/O Corporation
10525 Willows Road N.E.
C-46
Redmond, WA 98052
(206) 455-3990
Telex 320290
(Sales & Service)

NORTHERN CALIFORNIA

Data I/O Corporation
473 Sapena Court
Suite 4
Santa Clara, CA 95050
(408) 727-0641
Telex 352054
(Sales & Service)

SOUTHERN CALIFORNIA

Data I/O Corporation
14937 Ventura Blvd.
Suite 306
Sherman Oaks, CA 91403
(213) 501-3301
Telex 194701
(Sales)

Data I/O Corporation
2740 South Harbor Blvd.
Suite D
Santa Ana, CA 92704
(714) 979-3621
(Service)

EASTERN REGION ADMINISTRATIVE OFFICE

MAINE, MASSACHUSETTS, NEW HAMPSHIRE, RHODE ISLAND, VERMONT

Data I/O Corporation
Nashua Road
Route 101A
Amherst, NH 03031
(603) 889-8511 *(Sales)*
(603) 889-8513 *(Service)*
Telex 943431

NEW JERSEY, NEW YORK, LONG ISLAND, CONNECTICUT EXCLUDING UPSTATE NEW YORK

Data I/O Corporation
2171 Jericho Turnpike
Suite 230
Commack, NY 11725
(516) 499-0140 *(Sales)*
(516) 499-0335 *(Service)*
Telex 967846

MID ATLANTIC REGION ADMINISTRATIVE OFFICE

Data I/O Corporation
7720 Wisconsin Avenue
Suite 227
Bethesda, MD 20014
(301) 652-7240

CENTRAL REGION ADMINISTRATIVE OFFICE

Data I/O Corporation
3361 Successful Way
Dayton, OH 45414
(513) 236-6695
Telex 288315
(Sales & Service)

SOUTHERN REGION ADMINISTRATIVE OFFICE

Data I/O Corporation
1702 N. Collins Blvd.
Suite 110
Richardson, TX 75080
(214) 235-0044
(800) 527-0916 (Not Texas)
Telex 792474
(Sales)

Representatives

(Sales Only)

ARKANSAS, LOUISIANA, OKLAHOMA, TEXAS

USDATA
14241 Proton Road
Dallas, TX 75234
(214) 661-9633
Telex 910-860-5380

2400 Central Pwky.
Suite M
Houston, TX 77092
(713) 681-0200

8701 Shoal Creek Blvd.
Bldg. 1, Suite 104
Austin, TX 78758
(512) 454-3579

9820 E. 41st Street
Tulsa, OK 74145
(918) 622-8740

MICHIGAN, EASTERN KENTUCKY, OHIO, WEST VIRGINIA, WEST PENNSYLVANIA

Electro Sales Associates
851 East 222nd Street
Cleveland, OH 44123
(216) 261-5440

22126 Ford Road
Dearborn Heights, MI 48127
(313) 561-0045

1635 Mardon Drive
Dayton, OH 45432
(513) 426-5551

3740 Mount Royal Blvd
Allison Park, PA 15101
(412) 487-3801

UPSTATE NEW YORK

Martin P. Andrews
319 Mott Road
P.O. Box 443
Fayetteville, NY 13066
(315) 637-5291

KANSAS, MISSOURI, NEBRASKA, SOUTHERN ILLINOIS

Midtec Associates, Inc.
7702 Mize Road
DeSoto, KS 66018
(913) 441-6565

110 South Highway 67
Florissant, MO 63033
(314) 837-5200

ALABAMA, FLORIDA, GEORGIA, MISSISSIPPI, NORTH CAROLINA, SOUTH CAROLINA TENNESSEE

Pen Tech Associates
1398 Semoran Blvd.
Suite 106
Casselberry, FL 32707
(305) 645-3444

201 S.E. 15th Terrace
Suite K
Deerfield Beach, FL 33441
(305) 421-4989

Cherokee Center
Suite 21
627 Cherokee Street
Marietta, GA 30060
(404) 424-1931

Holiday Office Center
3322 Memorial Pkwy. S.W.
Huntsville, AL 35801
(205) 881-9298

1202 Eastchester Drive
High Point, NC 27260
(919) 883-9125

INDIANA, IOWA, WESTERN KENTUCKY, MINNESOTA, NORTHERN ILLINOIS, NORTH DAKOTA, SOUTH DAKOTA, WISCONSIN

Torkelson Associates
4940 Viking Drive
Minneapolis, MN 55435
(612) 835-2414

550 West Frontage Rd., RM 3052
Northfield IL 60093
(312) 446 9085

2346 S. Lynhurst
Room B101
Indianapolis, IN 46241
(317) 244-7867

2840 N. Brookfield Road
Brookfield, WI 53005
(414) 784-7736

ARIZONA, COLORADO, IDAHO, MONTANA, NEW MEXICO, NEVADA, UTAH, WYOMING

Zeus Incorporated
546 E. Portland
Phoenix, AZ 85004
1-800-528-4512
(602) 253-6101
TWX 910-951-1362

310 Val Verde, S.E
Albuquerque, NM 87108
1-800 525-4512
(505) 842-6633
TWX 910-989-1664

3333 Quebec Street
Suite 2950
Denver, CO 80207
1-800-528-4512
(303) 321-4246

1849 W. North Temple
Suite 377
Salt Lake City, UT 84116
1-800 528-4512
(801) 534-0500

SOUTHERN NEW JERSEY, DELAWARE, MARYLAND, EASTERN PENNSYLVANIA, VIRGINIA, WASHINGTON D.C.

Scientific Representatives, Inc.
496 North Kings Highway
Cherry Hill, NJ 08034
(609) 482-0059

9512A Lee Highway
Fairfax, VA 22031
(703) 385-0600

CANADA

Alan Crawford Associates, Ltd.
6503 Northam Drive
Mississauga, Ontario L4V 1J2
(416) 678-1500
Telex 06 968769

881 Lady Ellen Place
Ottawa, Ontario K1Z 5L3
(613) 722-7682
Telex 053 3600

7018 Cote De Liesse
St. Laurent, P.Q. H4T 1E7
(514) 731-8564
Telex 05-824944

1935-30th Avenue N.E.
Calgary, Alberta T2E 6Z5
(403) 230-1341
Telex 03-821186

3795 William Street
Burnaby, B.C. V5C 3H3
(604) 294-1326
Telex 04 54247

192 Joseph Zatzman Drive
Dartmouth, Nova Scotia B3B 1N4
(902) 463-9360
Telex 019 31604

15043A 118th Avenue
Edmonton, Alberta T5V 1H9
(403) 451-4893

Addresses on this list subject to change without notice.

DATA I/O

Programming systems for tomorrow...today

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual: _____

How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

Name _____

Company _____ Department _____ M/S _____

Address _____

City _____ State _____ Zip _____ Phone _____

Manual or Part No. _____

Warranty/Registration

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . YES ○ ○ NO
Did this equipment arrive intact, without loose parts or cable damage? . . . . . YES ○ ○ NO
Did the equipment operate on power-up? . . . . . YES ○ ○ NO
Did you attain adequate system performance? . . . . . YES ○ ○ NO
Were any electrical adjustments required? . . . . . YES ○ ○ NO
If you required assistance, was a local Data I/O representative contacted? . . . . . YES ○ ○ NO

Comments – _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____ Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

90 Day Warranty

Data I/O warrants that all equipment sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for 90 days. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect; if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to and from Data I/O's facility shall be borne on account of buyer.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCANTIBILITY AND THE WARRANTY OF FITNESS FOR PARTICULAR PURPOSE.

DATA I/O
Programming systems for tomorrow...today

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL FIRST CLASS Permit No. 24 Issaquah, WA 98027

Postage will be paid by:

DATA I/O Reader Comments

Director of Sales Support
P. O. Box 308
1297 Northwest Mall
Issaquah, WA 98027

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL FIRST CLASS Permit No. 24 Issaquah, WA 98027

Postage will be paid by:

DATA I/O Warranty/Registration

Service Manager
P. O. Box 308
1297 Northwest Mall
Issaquah, WA 98027

DATA I/O

Programming systems for tomorrow... today